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Fibre integrated circuits by a multilayered spiral architecture

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Zhen Wang[1,8], Ke Chen[1,8], Xiang Shi[1,8], Qinhao Du[1], Yulu Ai[1], Pengzhou Li[1], Li Yong[1], Xiao Sun[1], Ning Wang[1], Xuemeng Hu[2], Chen Lu[2], Chengqiang Tang[1], Liyuan Wang[1], Yuanyuan Zheng[1], Yichi Zhang[1], Hongyu Guo[1], Zhaofangzhou Pu[1], Xiaokun Wang[1], Yanan Zhang[1], Haibo Jiang[1], Yue Liu[1], Zhihang Tang[3], Lingsen You[4], Jue Deng[5], Renchao Che[6], Yue Gao[1], Songlin Zhang[1], Bingjie Wang[1], Xuemei Sun[1], Jiajun Qin[1], Ya Huang[1], Li Shen[4], Junbo Ge[4], Xiaoyang Zeng[2], Lin Chen[2], Peining Chen[1,7]✉ & Huisheng Peng[1]✉

Fibre electronic devices are transforming traditional fibres and garments into new-generation wearables that can actively interact with human bodies and the environment to shape future life[1–5]. Fibre electronic devices have achieved almost all of the desired functions, such as powering[6,7], sensing[8,9] and display[10,11] functions. However, viable information-processing fibres, which lie at the heart of building intelligent interactive fibre systems similar to any electronic product, remain the missing piece of the puzzle[12–15]. Here we fill this gap by creating a fibre integrated circuit (FIC) with unprecedented microdevice density and multimodal processing capacity. The integration density reaches 100,000 transistors per centimetre, which effectively satisfies the requirements for interactive fibre systems. The FICs can not only process digital and analogue signals similar to typical commercial arithmetic chips but also achieve high-recognition-accuracy neural computing similar to that of the state-of-the-art in-memory image processors. The FICs are stable under harsh service conditions that bulky and planar counterparts have difficulty withstanding, such as repeated bending and abrasion for 10,000 cycles, stretching to 30%, twisting at an angle of 180° cm^{-1} and even crushing by a container truck weighing 15.6 tons. The realization of FICs enables closed-loop systems in a single fibre, without the need for any external rigid and bulky information processors. We demonstrate that this fully flexible fibre system paves the way for the interaction pattern desired in many cutting-edge applications, for example, brain–computer interfaces, smart textiles and virtual-reality wearables. This work presents new insights that can promote the development of fibre devices towards intelligent systems.

The evolution of fibre electronic devices from traditional fibres to fibre devices with diverse functionalities has been witnessed in the past decades[16,17]. Following the development of any electronic product such as a smartphone or a computer, the future of fibre electronic devices necessitates the transformation of individually working fibre devices into intelligent fibre systems, aiming to meet the versatile interaction demands of large-scale applications[18,19]. Information processors such as integrated circuits or chips constitute the cornerstone of modern electronics. The same is true for fibre electronic devices; however, unfortunately, the missing piece to build fibre systems is an effective information processor in fibre form, which is necessary to seamlessly integrate multifunctional fibre devices for signal transmission, storage and processing[20–22]. The realization of fibre information processors is poised to overturn the present model of fibre systems, which heavily relies on external connection to rigid and bulky information-processing equipment[23–25]. This reliance is fundamentally at odds with the nature of fibre devices, which must be flexible, stretchable, twistable, lightweight and even weavable (Supplementary Note 3).

Different from conventional information processors made on rigid planar silicon substrates, the primary challenge in developing a viable fibre information processor lies in the need to integrate a large number of collaborative processing microdevices—such as transistors, resistors and capacitors—into elastic and thin fibres. This difficulty arises from the inherent constraints of fibres, including their soft, cylindrical geometry and limited surface area, which create substantial barriers to achieving the necessary integration density and forming reliable

[1]State Key Laboratory of Molecular Engineering of Polymers, Department of Macromolecular Science, Institute of Fiber Materials and Devices, and Laboratory of Advanced Materials, Fudan University, Shanghai, China. [2]School of Microelectronics, State Key Laboratory of Integrated Chips and Systems, Fudan University, Shanghai, China. [3]Academician Workstation for Smart Fiber Materials, Hunan Institute of Engineering, Xiangtan, China. [4]State Key Laboratory of Cardiovascular Diseases, Department of Cardiology, Zhongshan Hospital, Fudan University, Shanghai Institute of Cardiovascular Diseases, Shanghai, China. [5]Academy for Engineering & Technology, Fudan University, Shanghai, China. [6]Electron Microscopy Center, Fudan University, Shanghai, China. [7]Shanghai Academy of Artificial Intelligence for Science, Shanghai, China. [8]These authors contributed equally: Zhen Wang, Ke Chen, Xiang Shi. ✉e-mail: peiningc@fudan.edu.cn; penghs@fudan.edu.cn

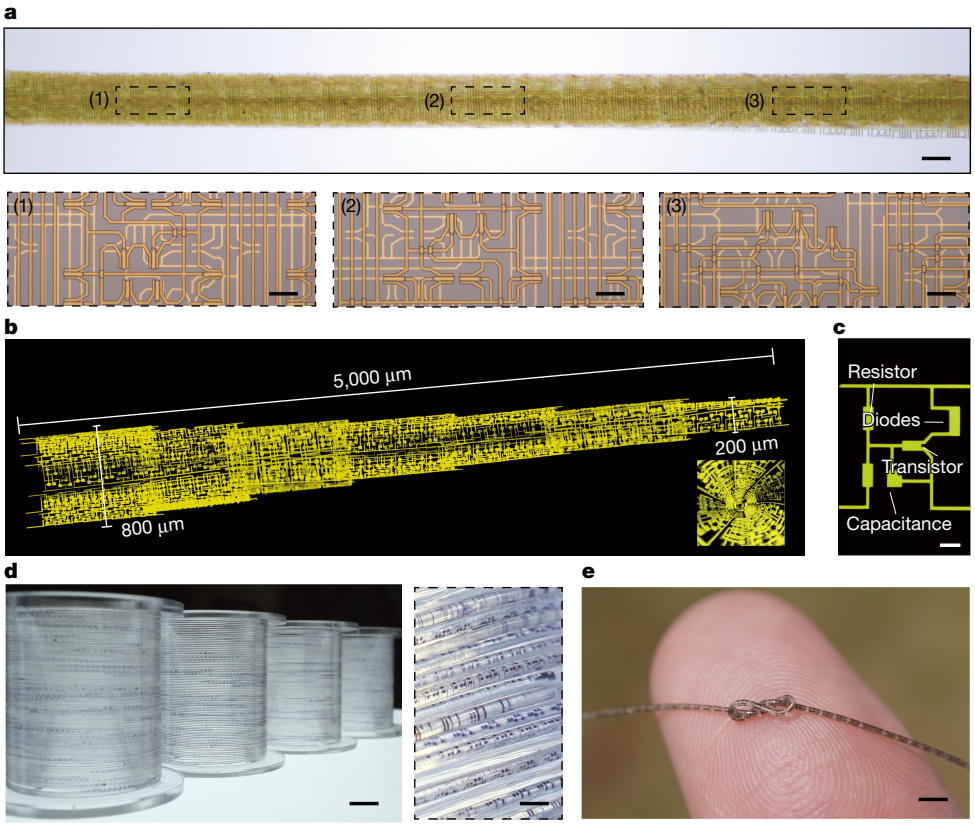

Fig. 1 | Photographs showing the structure of FICs. a, Photograph of a FIC with XOR circuits on the fibre surface (scale bar, 200 μm) and enlarged views (scale bars, 40 μm). (1), (2) and (3) show the uniformity of the circuits in the FIC. **b**, Reconstructed three-dimensional fluorescence photomicrograph showing the connectivity of the microdevices in a FIC. The circuit can be distributed 360° around the fibre circumference. **c**, Fluorescence photomicrograph showing an active driving circuit unit inside a FIC, suggesting that a wide variety of devices can be integrated into the fibre. Scale bar, 40 μm. **d**, Photograph of FICs being produced at a large scale. The enlarged photograph shows the continuity of circuits in the FICs. Scale bars, 1 cm (left); 1 mm (right). **e**, Photograph of a FIC being knotted and placed on a thumb, exhibiting the flexibility and structural integrity of the FIC. Scale bar, 2 mm.

interconnections required for meaningful computational functionality[26,27]. In our study, this limit was broken with a FIC by designing a multilayered spiral architecture, in which each layer had stretchable functional integrated circuits incorporated (Supplementary Note 1). This design enabled the creation of a stereoscopic spiral circuit architecture (Extended Data Fig. 1 and Supplementary Fig. 7), maximizing the radial space within the fibre and achieving a volumetric integration density an order of magnitude higher than that of methods confined to surface-level utilization[24].

The fabrication processes of FICs involve constructing functional modules on elastic polymer substrate, interconnecting them by means of lithography and assembling them into FICs using a modified rolling strategy (see Methods for details). The integration density of a FIC could be readily tuned by changing the lithography processing resolution, whereas FICs of various diameters and lengths could be obtained on demand by using substrates of different sizes (Extended Data Fig. 2 and Supplementary Note 6). To ensure the reliable performances of integrated circuits in the fibres, we implemented three key strategies in fabrication processes beyond traditional rolling methods[28]. First, we established a highly flat surface on polymer substrate to enhance circuit patterning precision and developed parylene encapsulation to provide solvent resistance (Supplementary Note 7). Second, we introduced a polydimethylsiloxane (PDMS) interlayer and a modulus heterostructure to mitigate mechanical stresses of circuits during deformations (Supplementary Notes 2 and 8). Third, to address device uniformity and reproducibility, we integrated an adhesive interlayer and a thickened edge into the FIC fabrication process, which improved layer adhesion and prevented irregular layer curing (Supplementary Note 9).

The interconnectivity among microdevices is crucial for their collaborative operation in performing computations within FICs, achieved through upper-layer connecting tracks (Supplementary Fig. 4). As shown in Fig. 1a, a 300-μm-diameter FIC was fabricated with exclusive-or (XOR) logic gate circuits arrayed along its longitudinal axis. XOR logic gates, which are fundamental building blocks for computational and error-correction circuits, were precisely implemented. The conducting circuit in the resulting FIC featured a line width of 5 μm, demonstrating a fabrication resolution superior to that achieved by typical printing or thermal-drawing methods in fibre devices[25,28,29]. The circuit interconnections showed high consistency and integrity, maintaining consistent resistances along the axial, radial and circumferential dimensions (Extended Data Fig. 6). To visualize the internal morphology, fluorescent molecules were used to label the circuits. The reconstructed three-dimensional images revealed that the circuits conformed well to the spiral geometry along the radial direction, without observable wrinkles or distortions (Fig. 1b and Extended Data Fig. 1a). The basic components of the integrated circuits—including resistors, capacitors, transistors and diodes—were precisely patterned and interconnected, forming a standard 1T1C circuit unit (Fig. 1c).

The scalability of interconnected FICs was demonstrated by extending their lengths from the centimetre to the metre level (Fig. 1d). A main difficulty in fabricating long FICs is that random wrinkles may form during the rolling process. To address this, we printed a 10-μm-width PDMS thickening layer at the initiating edge of the substrate, which serves as the core of the FIC (Extended Data Fig. 1d and Supplementary Notes 1 and 11). This design prevents stress concentration during rolling, enabling uniform and scalable fabrication of metre-scale FICs

using a custom-built machine (Fig. 1d and Extended Data Fig. 2a–c). Even in the innermost layer, the functional circuits were subjected to relatively low strains owing to the mechanically neutral layer design (Extended Data Fig. 5 and Supplementary Note 2). Furthermore, an adhesive interlayer was incorporated during the rolling process to improve the structural integrity and stability. This interlayer acts as a filler and ensures strong bonding between the rolled functional layers, effectively preventing delamination during FIC deformations (Fig. 1e and Supplementary Note 9).

As the core building component of information-processing circuits[30,31], transistors were densely incorporated into FICs to enable a robust signal-processing functionality. The FICs achieved an unprecedented integration density of 100,000 transistors per centimetre (Fig. 2a and Supplementary Note 12), reaching the industrial standard for very-large-scale integrated circuits[32]. The transistor was designed with a typical bottom-gate structure (Fig. 2b), exhibiting an on–off switching ratio of 10^7, a leakage current at the level of 10^{-10} A and a mobility of 1.13 $cm^2 V^{-1} s^{-1}$ (Fig. 2c and Supplementary Note 10), which are comparable with the state-of-the-art organic transistors[33,34]. The transistors exhibit consistent performance along the axial, radial and circumferential directions of the fibres, with performance variations remaining less than 8% (Fig. 2d and Extended Data Fig. 4g–i).

On the basis of the electrical performance and operational uniformity of the transistors, the FICs enable the implementation of various functional circuits for signal computation and manipulation. For example, FICs containing basic logic gates such as not-or (NOR) and not-and (NAND) gates exhibited stable response curves that closely aligned with theoretical truth tables (Fig. 2e–h). To demonstrate the computation potential of FICs, a logic XOR gate was fabricated using four NAND gates (Fig. 2i). This XOR gate accurately performed addition and subtraction operations, with the response properties confirming the collective functionality of the integrated transistors (Fig. 2j). Furthermore, the FICs could function as set-reset (RS) latch circuits, which are widely used in computers and digital systems for signal synchronization and timing control (Fig. 2k). The RS latch in the FIC exhibited electrical output responses consistent with theoretical predictions for sequential logic circuits (Fig. 2l).

As well as digital circuit functions, the FICs demonstrated the ability to achieve analogue circuit functionality, enabling direct communication with sensors and output devices such as radio frequency filters and waveform generators (Fig. 2m,n). This functionality was realized by integrating transistors with resistors and capacitors that offer adjustable performance and design flexibility (Supplementary Note 1 and Extended Data Fig. 10a,b). As an example, a waveform-generation circuit was designed on the basis of the electrical performance of transistors, which stably output a wave signal with a 1-s period and a 100-ms pulse width (variation of less than 5%; Fig. 2o). By integrating with an external 10-μF capacitor, the waveform generator achieved a performance comparable with the stimulus signal output capabilities of the commercial chips used in electrotherapy stimulation devices.

To address the demands for energy-efficient and area-efficient neural computation, organic electrochemical transistors (OECTs) were integrated into FICs, making use of their advantages of low-voltage operation and high sensitivity[35] (Extended Data Fig. 3a,b). The OECT unit demonstrated an on–off switching ratio of 10^6, a threshold voltage of −1.2 V and a hysteresis voltage of 1.02 V, which are comparable with those of state-of-the-art planar OECTs (Extended Data Fig. 4a–f). Neural computing functionalities were successfully achieved with the FICs (Extended Data Fig. 3d–h and Supplementary Note 5). For example, the FICs performed pattern-recognition tasks with high accuracy. The Olivetti Research Laboratory database recognition task was performed using a simulated OECT array, with each unit standardized on the basis of experimentally characterized OECT long-term potentiation[36–38]. After 1,000 learning epochs with 5,000 training images and 1,000 test images, the FIC achieved an average recognition accuracy of 99.8% (Extended Data Fig. 3g). This performance is on par with that of state-of-the-art in-memory image processors[39], highlighting the potential of FICs to meet the demands of learning and recognition applications.

The FICs were stable and durable enough to withstand various deformations that occur in real implantable or wearable applications, attributed to the modulus heterostructure within the FIC, featuring alternately distributed high-modulus parylene buffers and soft PDMS interlayers (Fig. 3a,b). To analyse this, a finite element method was used to simulate the strain distribution across the numerous components of a simplified FIC model. Simulation results showed that parylene buffer effectively dispersed strain to the elastic matrix, greatly reducing the local strain in the circuit during deformation (Fig. 3b). The effectiveness of this design had also been verified by systematic simulation analysis of realistic FIC configurations, showing no notable strain concentration of circuits that exceeded their threshold under severe fibre deformations, such as bending (1-mm bending radius), stretching (20%) and twisting (180° mm^{-1}) (Extended Data Fig. 7a and Supplementary Note 2). Experimentally, the mechanically heterogeneous design was also validated to ensure the stability and durability of the FICs under various deformations encountered in practical applications (Fig. 3c–i, Extended Data Figs. 7b–g and 8 and Supplementary Note 3). Notably, the FIC remained fully operational even after being crushed by a 15.6-ton container truck (Fig. 3c–e). The electrical properties of the FIC, including the on–off ratio and threshold voltage of transistors, remained stable (with <5% variation) during complex deformations such as bending (1-mm radius), twisting (180° cm^{-1}) and stretching (30% strain) (Fig. 3f–h). Moreover, the FICs retained more than 92% of their initial on–off ratio performances under practical wearing conditions (Extended Data Fig. 8). Even under 10 days of 10% stretching and 1,000 cycles of 40 °C thermal cycling, the FICs exhibited consistent resistance and current output, with variations of less than 6% and no circuit delamination observed (Supplementary Note 3). The FIC also demonstrated robust performance after 100,000 abrasion cycles (Fig. 3i) and 10,000 cycles of bending and stretching (Extended Data Fig. 7f,g). The electrical variations remained within 10%—a level of resilience that is difficult to achieve with traditional electronics using intrinsically rigid and brittle substrates such as quartz, mica or silicon. Furthermore, the FICs could continuously operate for 12 h with a maximum temperature less than 34.5 °C (Supplementary Fig. 29).

Efficient information processors are the key elements used to build intelligent fibre systems. Previously, fibre systems primarily depended on external bulky chips for signal processing and control[12]. This integration model inevitably led to challenges such as complex electrical interconnections, uncomfortable wearability and unsafe implantation[2,8,9]. FICs have enabled a new integration strategy for fibre systems by transferring closed-loop functions—including powering, sensing, information processing and display functions—into a single thin fibre (Fig. 4a,b, Extended Data Fig. 9 and Supplementary Notes 1 and 3). As a demonstration, Fig. 4b shows a 300-μm-diameter fibre system with different functional modules arranged in segments inside. The cooperative processing units process the raw signals from the sensing inputs and then control the display outputs after logical judgement. To address the powering demand, thermoelectric energy-harvesting and energy-storage units were integrated, with the thermoelectric units generating electricity to charge the energy-storage units[40] (Extended Data Fig. 10). The rechargeable energy-storage module could achieve adjustable voltage output ranging from 1.5 to 60 V by connecting different energy-storage modules in series (Extended Data Fig. 10c–h and Supplementary Note 14), well satisfying the requirements of the functional modules in the FICs. The organic light-emitting diode (OLED) displaying module achieved a brightness of 10^4 cd m^{-2} (Extended Data Fig. 9d and Supplementary Note 13), effectively meeting the requirements for interactive applications. Its present efficiency reached 2.55 cd A^{-1} at a luminance of 2,000 cd m^{-2}, matching the performance of planar counterparts[41,42]. Each pixel could be individually controlled

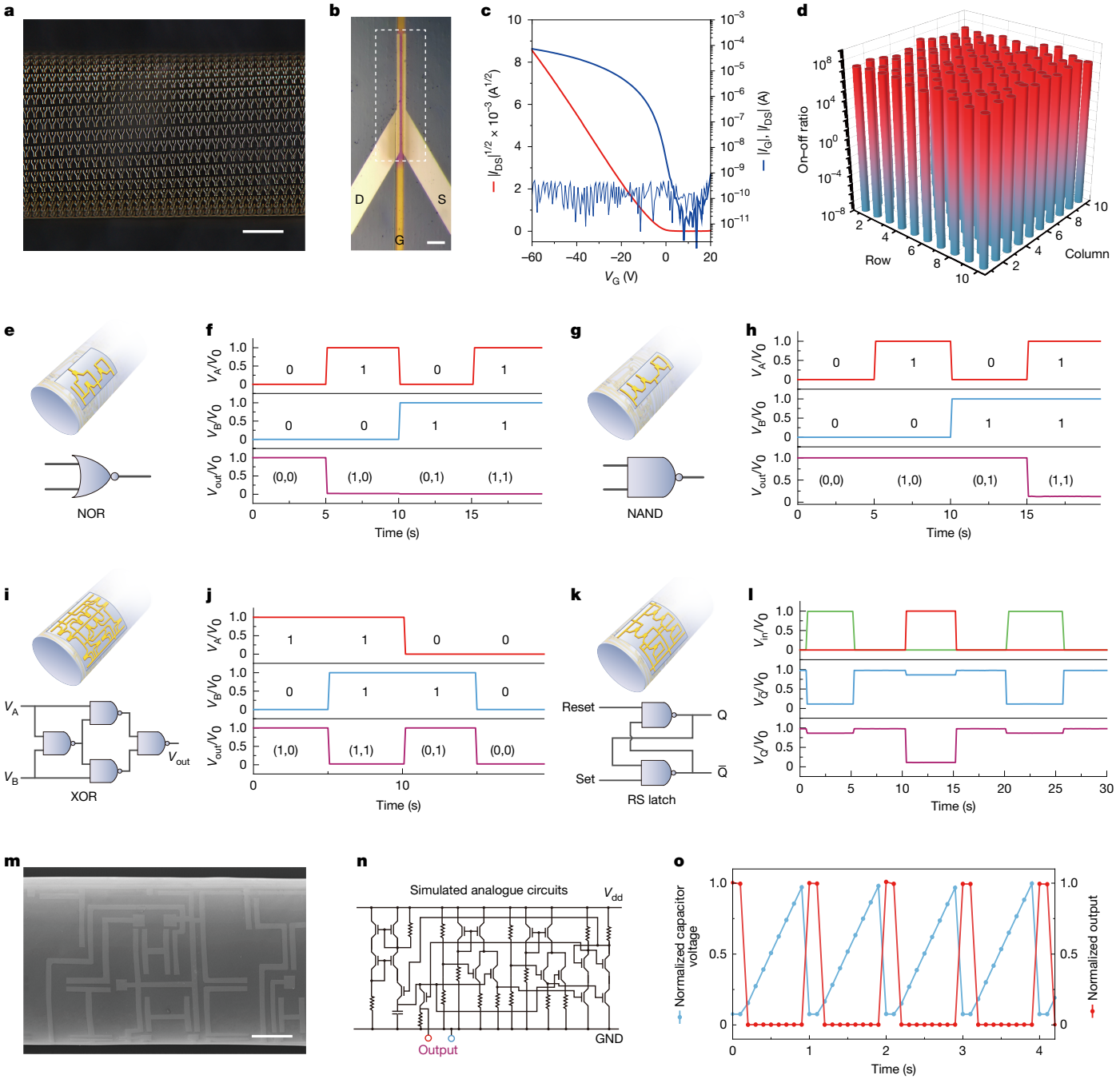

Fig. 2 | Electrical properties of transistors and logic circuits in FICs. **a**, Demonstration of a FIC with an integration density of 100,000 transistors per cm. Scale bar, 100 µm. **b**, Optical microscopy photograph of the tested transistor in a FIC. White dashed box indicates semiconductor. D, drain; G, gate; S, source. Scale bar, 80 µm. **c**, Transition curve of transistors in a FIC, suggesting the high on–off ratio of the transistors. I_{DS}, drain–source current; I_G, gate current. **d**, Columnar statistics of the on–off ratio of 100 transistors prepared in the same batch, showing the homogeneity of the electrical properties. **e**, Schematic of the NOR gate circuit in a FIC. **f**, Voltage output of the NOR gate circuit in a FIC for the corresponding input voltage. **g**, Schematic of the NAND gate circuit in a FIC. **h**, Voltage output of the NAND gate circuit in a FIC for the corresponding input voltage. **i**, Schematic of the XOR gate circuit in a FIC. **j**, Voltage output of the XOR gate circuit in a FIC for the corresponding input voltage. **k**, Schematic of the RS latch circuit in a FIC. **l**, Voltage output of the RS latch circuit in a FIC for the corresponding input voltage. **m**, Scanning electron microscopy image of an analogue circuit in a FIC. Scale bar, 100 µm. **n**, Schematic of the simulated analogue circuit in a FIC. GND, ground; V_{dd}, drain supply voltage. **o**, Statistical diagram of the simulated analogue circuit output for the actual electrical test results of transistors in integrated circuits.

through active matrix driving on the basis of the transistor array circuits (Fig. 4c). The independent operation of FICs without external control units was successfully realized, enabling users to regulate the light emission of OLED modules by simply touching the integrated sensing point in the system (Extended Data Fig. 9e,f, Supplementary Video 1 and Supplementary Note 15).

The fibre systems demonstrated skin-like softness, with a bending stiffness of 10^{-3} µN m^2 (Supplementary Fig. 41), ensuring their seamless compatibility with the biological tissues[43]. This characteristic makes the system highly suitable for both implantable and wearable applications. As a proof of concept, the capability of our FICs to act as a closed-loop neural probing system for the benefit of future brain–computer

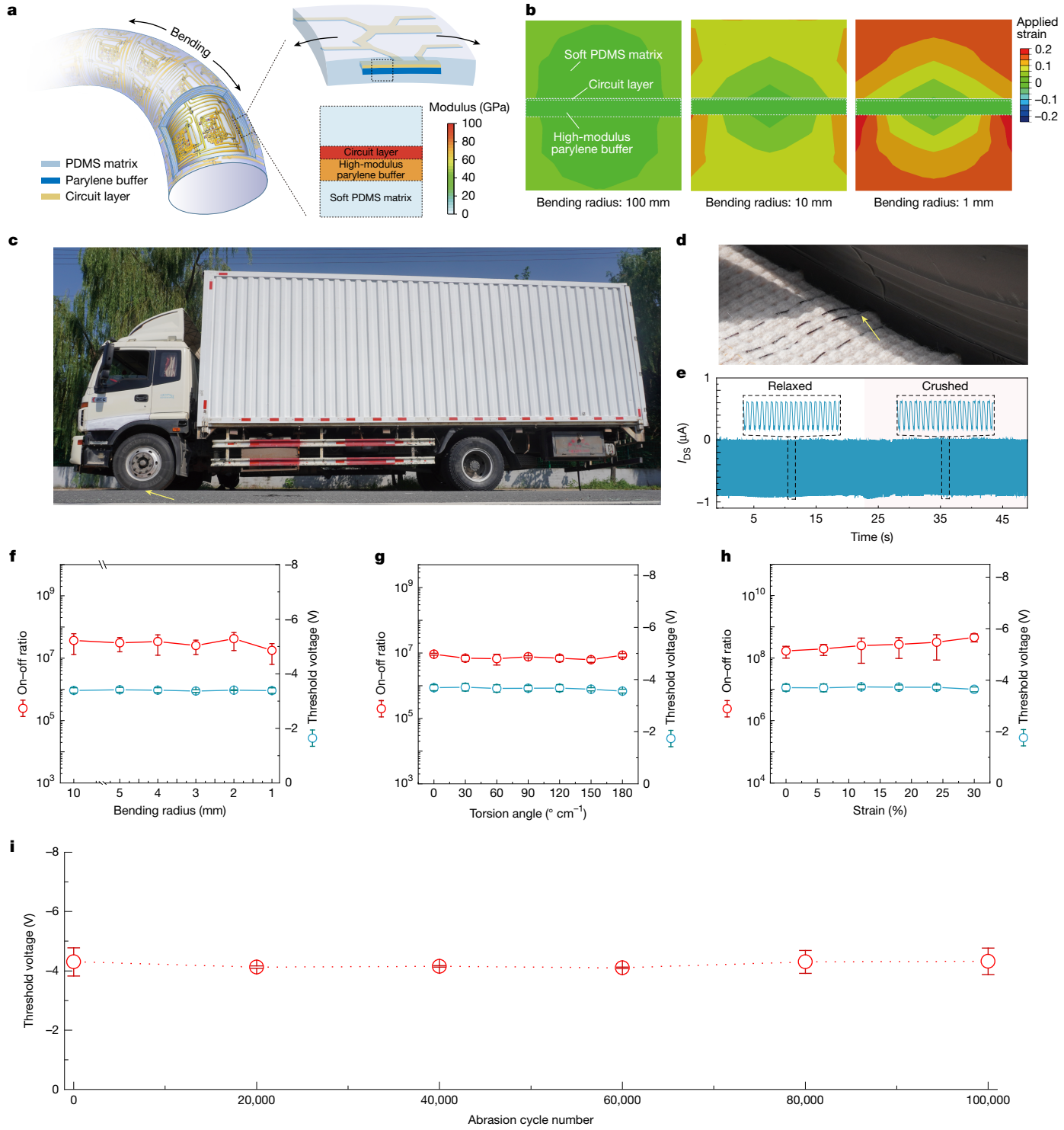

Fig. 3 | Stability and durability of FICs. a, Schematic showing the modulus heterostructure design abstracted into a basic unit incorporates alternately distributed high-modulus parylene buffer and soft elastic interlayer. **b**, Finite element simulation results during fibre bending showing that the parylene layer well protects the circuit layer by dispersing strain into the elastic matrix. **c**, Photograph showing FICs being crushed by the front wheel of a container truck weighing 15.6 tons. **d**, Zoomed-in photograph showing the FICs being crushed by the front wheel of the container truck without mechanical failure. **e**, Frequency response performance of the device, which remains consistent before and after crushing. **f**, Statistical diagram of the on–off ratio and threshold voltage of transistors in FICs during bending with different radii. **g**, Statistical diagram of the on–off ratio and threshold voltage of transistors in FICs during twisting with different torsion angles. **h**, Statistical diagram of the on–off ratio and threshold voltage of transistors in FICs during stretching with different strains. **i**, Statistical diagram of the threshold voltage of the transistors in fibres during 100,000 abrasion cycles. Error bars are standard deviations of the results from at least four samples.

interfaces was demonstrated. Conventional neural probes typically rely on rigid external signal preprocessing circuits to achieve high signal-to-noise ratios in sensing outputs[8,9]. Our fibre system can efficiently avoid this issue by integrating high-density electrode arrays with corresponding in situ signal-processing circuits as preprocessing units (Fig. 4d). We successfully demonstrated 16-channel signal

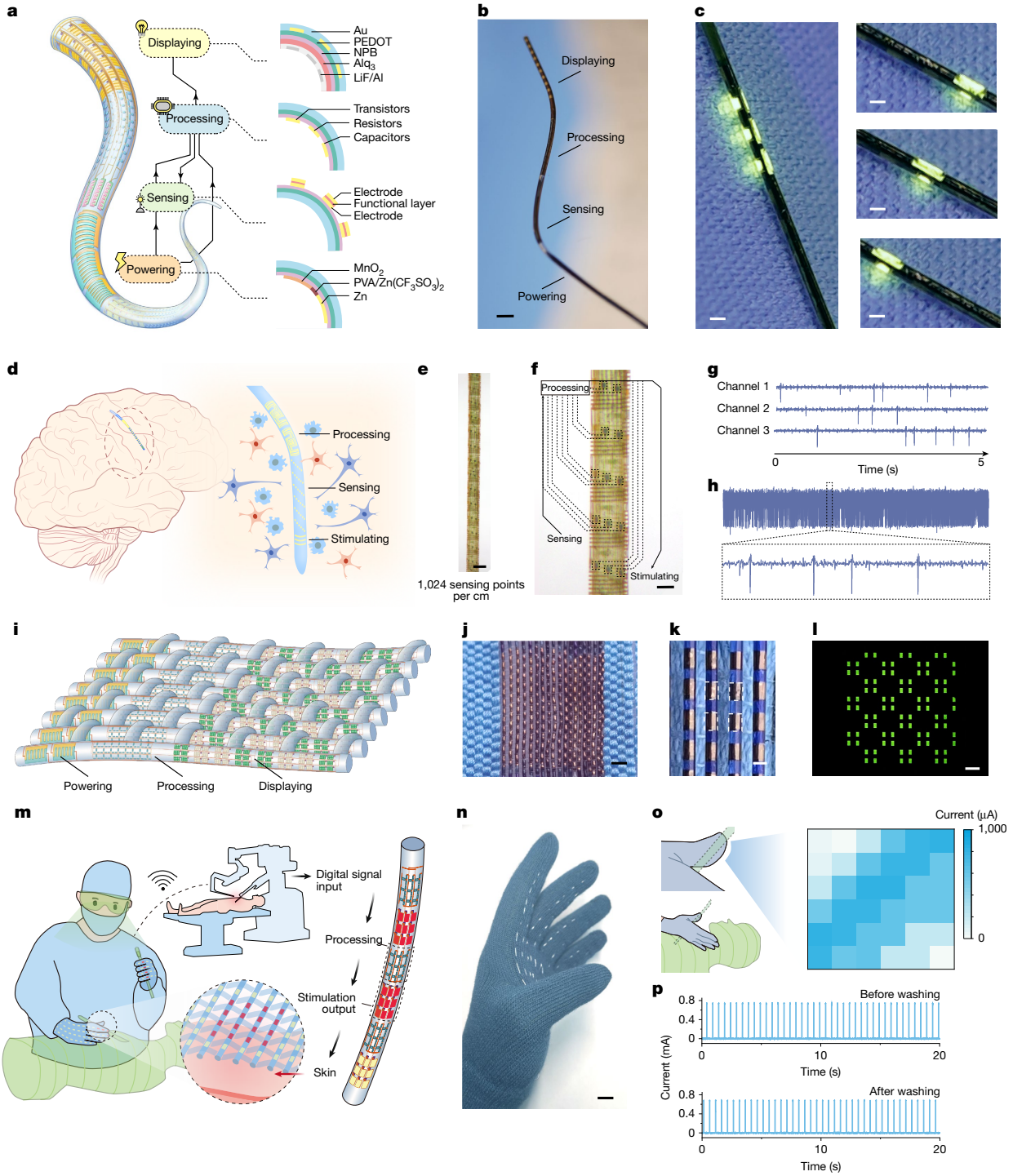

Fig. 4 | Integration and application of intelligent fibre systems. **a**, Schematic showing the structural design of a closed-loop intelligent fibre system in which several functional modules are seamlessly integrated. The powering module included both energy-harvesting and energy-storage units. NPB, *N*,*N*′-bis(naphthalen-1-yl)-*N*,*N*′-bis(phenyl)-benzidine; PEDOT, poly(3,4-ethylenedioxythiophene). **b**, Photograph showing the intelligent fibre system with different functional modules integrated in segments. Scale bar, 800 μm. **c**, Photograph showing that the display pixels could be individually controlled through circuits integrated in the intelligent fibre system. Scale bars, 300 μm. **d**, Schematic showing that the intelligent fibre system allows integration of high-density sensing arrays with in situ signal-processing circuits and stimulation electrodes. **e**, Photograph showing a 50-μm-diameter FIC integrated with a 1,024-channel-per-cm sensing electrode array. Scale bar, 50 μm. **f**, Zoomed-in photograph showing the sensing/stimulating electrode around the intelligent fibre system. Scale bar, 25 μm. **g**, Neural signal obtained from three randomly selected channels. **h**, Zoomed-in diagram of the neural signal collected from in situ signal-amplification circuits. **i**, Schematic showing that an intelligent fibre system could be easily woven into integrated electronic textiles. **j**, Photograph showing the pixel display textile woven from active-matrix-driving-circuit-integrated fibre systems. Scale bar, 1 mm. **k**, Zoomed-in photograph showing the pixel pitch of the pixel display textiles. Scale bar, 500 μm. **l**, Photograph showing the ability of pixel-display textiles to display complex images. Scale bar, 500 μm. **m**, Schematic showing intelligent-fibre-system-woven smart textiles as flexible haptic interfaces enabling fine touch and free movement in virtual-reality scenarios (for example, remote surgery). **n**, Photograph showing haptic gloves woven from an intelligent fibre system. Scale bar, 8 mm. **o**, Heatmap showing the designable distribution of the electrical stimulation intensity on the surface of the haptic glove. **p**, Statistical diagram of the stimulus output from the haptic gloves before and after washing.

collection and showcased the potential for scaling up to 1,024-channel integration using in situ amplification circuits within a single fibre (Fig. 4e,f and Supplementary Note 16). Neural signals were transmitted by means of 15-μm × 15-μm sensing electrodes and processed in situ by the amplifier circuits of the FICs, eliminating potential transmission interference in electrodes. The Food and Drug Administration (FDA)-approved materials were used in this fibre integrated system, such as the electrode and polymer substrate materials[44]. Biocompatibility was rigorously validated through systematic tests, including platelet aggregation assays conducted in porcine blood for 2 weeks and inflammatory response assessment at 12 weeks post-implantation (Supplementary Note 4). The collected neural signals remained stable with a high signal-to-noise ratio after 8 weeks of implantation, showing no substantial signal loss or attenuation in signal strength (Supplementary Fig. 40). By making use of in situ signal amplification, neural signals achieved a high signal-to-noise ratio of 7.5 dB (Fig. 4g,h and Supplementary Note 16), demonstrating potential to replace commercial external signal-acquisition devices.

The FIC-enabled fibre system also opens possibilities for fully flexible, integrated smart textiles. Smart textiles are considered the ultimate goal of wearables, with an evaluated market value of 2 trillion euros over the next decade[45], but face the challenge of how to realize fully flexible and highly integrated systems[12,23]. Without the need for external processors, our FIC-enabled fibre system can be easily woven with a transparent wrap (nylon yarn) to create an electronic textile measuring 20 cm × 10 cm (Fig. 4i). Such FICs could serve as front-end processing units to greatly enhance the controllability and wearing comfort of smart textiles. For example, by using integrated active-matrix-driving circuits within a FIC, we can achieve a pixel display within a textile (Fig. 4j,k). This textile could display images on demand (Fig. 4l), with each pixel individually controllable without interference from other pixels in the same row or column. This display textile with control circuits showed a power consumption of 5 mW per pixel, comparable with commercial light-emitting diode displays. Moreover, FIC-integrated smart textiles can serve as fully flexible, interactive interfaces for virtual-reality applications. Traditional wearable haptic interfaces for virtual reality rely heavily on silicon-based signal-processing equipment, thus falling short in accurate and detailed signal acquisition/output owing to their loose fit with the irregular and soft surface of skin[46,47]. This issue is greatly intensified in situations requiring fine touch and movement, such as remote surgery. By comparison, our FIC-woven smart textile is fully flexible and breathable, similar to normal fabrics, thus enabling haptic interfaces for smooth and natural interactions between users and virtual environments (Fig. 4m). Specifically, a stimulation array integrated with corresponding one-to-one driving circuits within a FIC was woven into flexible haptic gloves (Fig. 4n and Supplementary Fig. 52). Each stimulation point in the gloves could be individually controlled by input signals, allowing differentiation of fine haptic patterns on the fingers (Fig. 4o). The stimulation current for each point was programmable and controllable. Furthermore, these FIC-woven textiles were durable across various application environments. The stimulation current remained stable, with a slight variation even after machine washing (Fig. 4p).

In summary, we have presented a FIC with high microdevice-integration density and signal-processing capacity, bridging the gap between individually working fibre devices and closed-loop functional fibre systems (Supplementary Note 18). The FIC-enabled fibre systems are fully flexible, similar to normal polymer yarns, and could work as a new efficient platform to change the ways in which people interact with electronics. To further boost computational performance, the FIC architecture can integrate more high-performance processing components, such as 2D transistors, thereby extending its potential for more advanced computing applications. For lab-to-fab transition and commercialization of FICs, it is important to further make scalable production by drawing on the manufacturing technology of fibre electronics[1,5], establish regulatory frameworks by referring implantable fibre electronics, extend long-term stability in vivo and deepen the biosafety assessment according to specific clinical requirements.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-025-09974-0.

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Methods

Fabrication of FICs

This section outlines the brief fabrication workflow for FICs, encompassing the fabrication of key components. More detailed fabrication protocols, including the patterning of several functional modules, implementation of interconnections and the spiral rolling process, are provided in Supplementary Note 1.

Preparation of substrate with parylene buffer. The fabrication of both top-gate and bottom-gate flexible transistors began with the preparation of a flexible substrate. First, a layer of PDMS-601 (weight ratio 9:1, Wacker Chemie AG) was spin-coated onto a polyethylene terephthalate sheet (Shenzhen Dongsheng Plastic Products Co., Ltd.) at 5,000 rpm for 120 s, followed by curing under ultraviolet (UV) irradiation for 1 h to achieve cross-linking. The cured PDMS surface was then treated with oxygen plasma (75 W, 10 Pa) for 3 min using a reactive ion etching system (Trion T2, Trion Technology) to improve surface uniformity and adhesion. Subsequently, a high-modulus parylene buffer layer was deposited onto the plasma-treated PDMS through chemical vapour deposition (CVD) using a parylene coater (Specialty Coating Systems, PDS 2010, KISCO Co.), providing mechanical support for subsequent device layers.

Fabrication of top-gate transistors. For top-gate transistors, the first step after depositing the parylene buffer layer was patterning the source and drain (S/D) electrodes using 50-nm-thick gold (Au). This patterning process involved four key steps: (1) thermal evaporation of 50-nm Au onto the parylene buffer layer at a rate of 0.5 Å s^{-1}; (2) spin-coating of S1813 photoresist at 2,000 rpm for 20 s, followed by annealing at 60 °C for 180 s to remove solvent, exposure using a direct-write optical lithography system (MicroWriter ML3, Durham Magneto Optics Ltd.) at a dose of 135 mJ cm^{-2}, development in a commercial photoresist developer (Jiangyin Jianghua Microelectronic Materials Co., Ltd.) for 30 s, rinsing with deionized water and drying with nitrogen (N_2) gas; (3) etching of the unprotected Au regions in an etchant solution (15 wt% KI and 3 wt% I_2 in deionized water) for 10 s, followed by deionized water rinsing and N_2 drying; (4) removal of the remaining S1813 photoresist by soaking the sample in acetone for 20 s. After defining the S/D electrodes, a 20-nm-thick pentacene layer (TCI Shanghai) was thermally evaporated as the organic semiconductor layer at a controlled rate of 0.3 Å s^{-1} using an organic-metal vacuum thermal evaporation system (FS380-S8, Suzhou Fangsheng Optoelectronic Co., Ltd.). A parylene dielectric layer was then deposited by CVD using 0.75 g of parylene precursor (Specialty Coating Systems, PDS 2010, KISCO Co.), followed by patterning of the 50-nm-thick Au gate electrode through the same lithographic etching process used for the S/D electrodes. To pattern the parylene buffer layer, dielectric layer and pentacene semiconductor layer, the sample was subjected to oxygen plasma treatment for 10 min, with the prefabricated Au electrodes acting as a mask to protect the active device regions. Etching was conducted at 150-W power with 10 sccm oxygen flow. To prevent overheating, etching was performed in cycles of 1 min etching and 2 min rest. After a total plasma treatment for 10 min, no obvious bubbling or delamination of Au on parylene occurred.

Fabrication of bottom-gate transistors. Bottom-gate transistors shared the same initial PDMS substrate and parylene buffer layer preparation steps as the top-gate devices. After depositing the parylene buffer layer, the 50-nm-thick Au gate electrode was patterned on the structured parylene buffer layer using the Au lithographic etching process. A parylene dielectric layer was then deposited using 0.75 g of parylene precursor through CVD, after which the 50-nm-thick Au S/D electrodes were patterned on the dielectric layer using the same Au patterning process. A 20-nm-thick pentacene semiconductor layer was thermally evaporated onto the S/D electrodes at 0.3 Å s^{-1} (FS380-S8, Suzhou Fangsheng Optoelectronic Co., Ltd.) and 0.8 g of parylene was further deposited to assist in semiconductor patterning. The semiconductor patterning process involved: (1) thermal evaporation of 60-nm Cu onto the parylene layer at 0.5 Å s^{-1} and patterning by lithography; (2) oxygen plasma treatment (75 W, 10 Pa) for 22 min to simultaneously etch the parylene and underlying pentacene in unmasked areas; (3) immersion in $FeCl_3$ solution for 30 s to remove excess Cu, followed by deionized water rinsing and N_2 drying. After completing all device layers, the blank sample regions were cut off and the device layer was spirally wound to fabricate the FIC.

Interconnection of modules in FICs. The interconnecting process began at the gap between two electrodes of different functional modules. First, parylene (0.8 g) was deposited as an insulating layer using CVD. Then, a 150-nm-thick Cu sacrificial layer was thermally deposited at a rate of 0.6 Å s^{-1}, followed by S1813 photoresist spin-coating at 2,000 rpm for 20 s and annealing at 60 °C for 180 s. Next, the photoresist was exposed to 365-nm i-line at a dose of 135 mJ cm^{-2}, developed in photoresist developer for 30 s, rinsed with deionized water and dried with N_2. After that, the Cu layer was patterned by etching in $FeCl_3$ solution and S1813 photoresist was removed in acetone for 20 s. Subsequently, 150-W O_2/N_2 plasma etching was carried out for 360 s to expose underlying gold connection points. The Cu sacrificial layer was then removed using $FeCl_3$ solution. 50-nm Au was thermally deposited at a rate of 0.5 Å s^{-1} to connect the two electrodes. The S1813 photolithography process was repeated to further pattern Au connections: spin-coating, baking, UV exposure and development were followed by Au etching in a solution (15 wt% KI and 3 wt% I_2 in deionized water). The remaining S1813 photoresist was removed in acetone for 20 s. Finally, 150-W O_2/N_2 plasma etching was performed for 360 s to remove excess parylene.

Rolling assembly of FICs. Individual functional modules were initially fabricated on PDMS substrate incorporated with a parylene buffer layer. Subsequently, in-plane interconnections were realized through upper-layer connecting tracks. A 10-μm-width PDMS thickening line was printed at the initiating edge of PDMS substrate before rolling up, which could locally increase the bending stiffness and inhibit the formation of wrinkles. To avoid layer delamination during deformation, a semi-cured PDMS layer (PDMS-601, weight ratio 9:1, Wacker Chemie AG, precured with 50 °C for 1.5 min) was deposited at the top of the film. Finally, the excess substrate was cut off and the sample was spirally wound with a speed of 0.2 cm per second to form a FIC by a customized rolling machine. The semi-cured layer was subsequently fully cured with 50 °C for 5 min to ensure reliable adhesion between layers.

Fabrication of fibre systems

The fabrication process of close-looped fibre systems began with the creation of lower circuits integrated with transistor units, along with electrodes for OLEDs, resistors, sensors and batteries by lithography. Subsequently, OLED modules were fabricated, in which layer patterning was achieved using mask template. Sensor units were then patterned using mask template. Next, upper circuits for interconnection were fabricated through lithography. Finally, resistor and energy-storage modules were fabricated and patterned through a combination of a mask template and printing. After completing all device layers, the blank sample regions were cut off and the device layer was rolled to fabricate the fibre system.

Fabrication of the displaying textile

The weaving operation of the display textile was conducted on a rapier loom (Tong Yuan Textile Machinery Co., Ltd.). The displaying fibre system could be easily woven with highly transparent wrap (nylon yarn) to form an electronic textile measuring 20 cm × 10 cm (length × width).

The size of each display pixel in the fibre system was designed to match the textile structure and pixels were arranged between the interweaving points of the textile during weaving. To interconnect FICs within textiles, the electrodes (micro contact pads) of each FIC can be directed onto an extended tab located on the fibre side. Polyimide adapters could then be used to establish point-to-point interconnection of the corresponding electrodes between FICs. Pixel displaying of the above textile was achieved by a typical driving circuit with every input port being connected to the corresponding external digital input.

Morphological characterizations

Optical images were captured by an Olympus EX51 optical microscope and a digital camera (Sony A6000). Fluorescence photographs were taken by a Nuohai LS-18 light sheet microscope. The microstructure and morphology of FICs were characterized using a cryo field-emission scanning electron microscope (Zeiss FE-SEM Ultra 55 operated at 3 kV) equipped with an energy-dispersive spectrometer detector.

Electrical characterizations

The electrical characteristics of transistors in FICs and fibre systems were measured using a probe station in an ambient environment connected to a Keysight 1500A parameter analyser. Characterizations of the circuits were also performed using the probe station. The circuits were characterized using the Keysight 1500A parameter analyser coupled to Keithley 2612B source meters. The voltage–light intensity curves for the OLED module in FICs were measured with a PR-680 luminance meter from Photo Research Inc. and a Keithley 2400 source meter. Electrical and electrochemical sensors were characterized by an electrical workstation (CHI660E, CH Instruments, Inc.) and a Keithley 2400 source meter. The Seebeck coefficients of FICs were measured by a custom-built set-up, which incorporated two Peltier elements positioned at both ends of the fibre to create a temperature difference. An infrared thermal camera (FOTRIC 226), mounted vertically above the fibre, was used to record the temperature difference (ΔT). Furthermore, a Keithley 2612B source meter was used to measure the voltage difference (ΔV) generated at both ends of the fibre. The Seebeck coefficient was calculated by

$$S = -\frac{\Delta V}{\Delta T}$$

All data related to the functional stability of FICs are shown as mean corrected values ± standard deviation (s.d.) of at least four independent experiments unless otherwise stated. We carried out graphing of the data using Microsoft Office Excel, Origin 2024 and Adobe Illustrator. The results are presented as the mean s.d.

Verification of the fidelity of the sensors of FICs in vivo

All of the animal experimental procedures were approved by the Ethics Committee of Fudan University (approval number SYXK2020-0032) and the international ethical guidelines and the National Institutes of Health Guide concerning the Care and Use of Laboratory Animals were strictly followed. A 2 × 10-pin connector was used for the adapter of fibre neural electrodes and connected by silver glue. In accordance with established protocols, flexible PI adapters were used to facilitate the interfacing between the fibre channels and the 2 × 10-pin connector. To reduce electromagnetic interference, the joint was sealed using silicone rubber. A viscous solution was formed by adding gelatin to water, with the gelatin constituting a 30% mass fraction of the mixture, and then stirring the mixture at 159 °C. For assistive implantation, gelatin fibres with a diameter of 10 μm were fixed on the connector, paralleling the FIC-enabled fibre system. At 120 °C, polyethylene glycol 4000 was melted and used to bond the materials together. Before implantation, they were disinfected using UV radiation on a clean bench. The fibre systems were tested in mice (ICR, 6 weeks old, Shanghai SLAC Laboratory Animal Co., Ltd.) housed in an ordinary animal room (12-h light/dark cycle, 22 °C, food and water ad libitum). Surgeries were conducted on deeply anaesthetized mice, which were positioned in a stereotactic frame (RWD). Before the surgery, the mice were pretreated with atropine sulfate (0.1 mg kg^{-1}, intraperitoneally) and anaesthetized with chloral hydrate (400 mg kg^{-1}). Subsequently, the scalp was removed using scissors. An electric drill was used to create openings in the skull at the implantation sites. The adapter, equipped with electrodes, was then loaded into an FHC hydraulic micro-positioner. The skull was drilled with a hole about 2 mm in diameter with the following stereotaxic coordinates: anteroposterior, 4.6 mm; mediolateral, 0.8 mm for the mitral cell layer and anteroposterior, −4.7 mm; mediolateral, 0.5 mm for the dlPAG layer. A sterile syringe needle was used to gently peel away the dura mater. On the opposite side, a flat-head screw was securely fastened to serve as the ground and reference electrode. Electrodes were implanted at a depth of 200 μm below the cortex. The electrophysiological recording was performed immediately. The raw data were collected through Blackrock Microsystems. Raw data were preprocessed through a high-pass filter with a passing frequency range of 800–5,000 Hz. We performed offline analysis using Spike2 (CED).

Washing test of the fibre system

Accelerated washing tests (approximately equal to five typical home launderings) were performed in a standard washing machine (SW-12E, Nantong Hongda Experimental Instrument Co., Ltd.) following the ISO 105-C10:2006 and AATCC 61-2013 international standards for fabric washing. The load information includes: a 4-cm × 10-cm section of the haptic fabric, 200 g of water and 0.5 wt% liquid detergent. Before washing, a total of ten steel balls (6 mm in diameter) were added into the washing containers. The washing process was conducted with a temperature of 60 °C, a duration of 30 min and a stirring speed of 1,000 rpm. After the washing test, the textiles were rinsed under flowing water and dried at 50 °C for 1 h.

Calculation of bending stiffness

To calculate the bending stiffness (D), a fixed boundary condition was set as one of the ends parallel with the bending direction and a small vertical displacement, d, was added on the other end. The bending stiffness can be defined as:

$$D = EI$$

in which E and I are the elastic modulus and moment of inertia, respectively. In our test, all fibres were selected to have a circular cross-section. For a circular cross-section of diameter d, the moment of inertia is:

$$I = \frac{\pi d^4}{64}$$

Finite element simulation of FICs

The entire finite element model is divided into three components; the model comprises a total of 205,950 nodes and 180,753 elements. Specifically, PDMS and parylene are modelled with solid elements of an eight-node linear brick, reduced integration, hourglass control, Au is represented by membrane elements of a four-node linear membrane, reduced integration, 50-nm thickness and the curled core cylinder is simulated as a discrete rigid body using elements of a four-node three-dimensional rigid quadrilateral.

For contact properties, normal behaviour is defined as hard contact to prevent penetration between interacting components, whereas tangential behaviour adopts the penalty friction formulation with a friction coefficient set to 0.3. To ensure the stability and accuracy of the transient analysis, small time steps are implemented, with an initial time step of 0.001 s, a minimum time step of 1×10^{-5} s and a maximum time step of 0.02 s.

The mechanical properties of each material in the model are as follows: Au has a density of 1.932×10^{-8} t mm^{-3}, an elastic modulus of 75,000 MPa, a Poisson's ratio of 0.4 and a yield strength of 500 MPa; parylene has a density of 1.289×10^{-9} t mm^{-3}, an elastic modulus of 2,900 MPa, a Poisson's ratio of 0.35 and a yield strength of 100 MPa; PDMS has a density of 9.65×10^{-10} t mm^{-3}, an elastic modulus of 2 MPa and a Poisson's ratio of 0.4, with no yield strength listed—this is because PDMS typically exhibits hyperelastic behaviour within the analysed deformation range and does not undergo plastic yielding under the applied loads in this study.

Reporting summary

Further information on research design is available in the Nature Portfolio Reporting Summary linked to this article.

Data availability

The data that support the findings of this study are available from figshare at https://figshare.com/s/49d5ed422b56a22dda21. Source data are provided with this paper.

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Author contributions H.P. and P.C. conceived and designed the research project. Z.W., X. Shi, K.C. and Q.D. performed the experiments on the FICs. Y.A. and Z.W. performed the simulation. X.H. and C.L. performed the simulation on transistors. L. Yong performed the experiments on sensing modules. P.L., H.J. and Y. Zhang performed the experiments on energy-storage modules. N.W. and Y. Zheng performed the experiments on energy-harvesting modules. K.C. and X.W. performed the experiments on displaying modules. L. You, Xiao Sun, L.W. and C.T. performed the biocompatibility and immunological experiments. Z.W., H.G., Z.P., Yichi Zhang and Q.D. performed the durability test. Z.W. and X. Shi analysed the data. Z.W., Y.L., Z.T., J.D., R.C., Y.G., S.Z., B.W., Xuemei Sun, J.Q., L.S., J.G., X.Z., L.C., Y.H., P.C. and H.P. discussed the data and wrote the paper.

Competing interests The authors declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to Peining Chen or Huisheng Peng.

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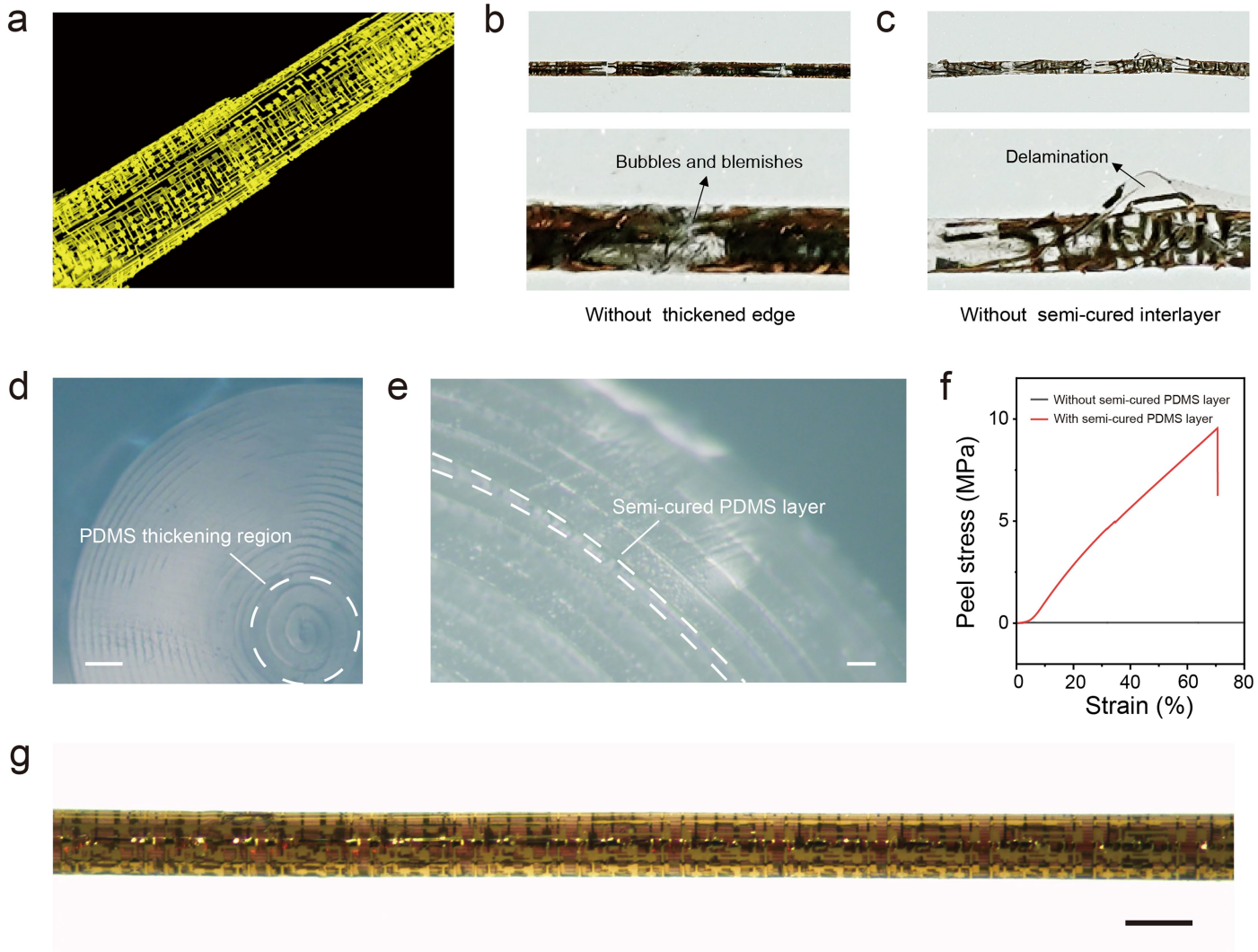
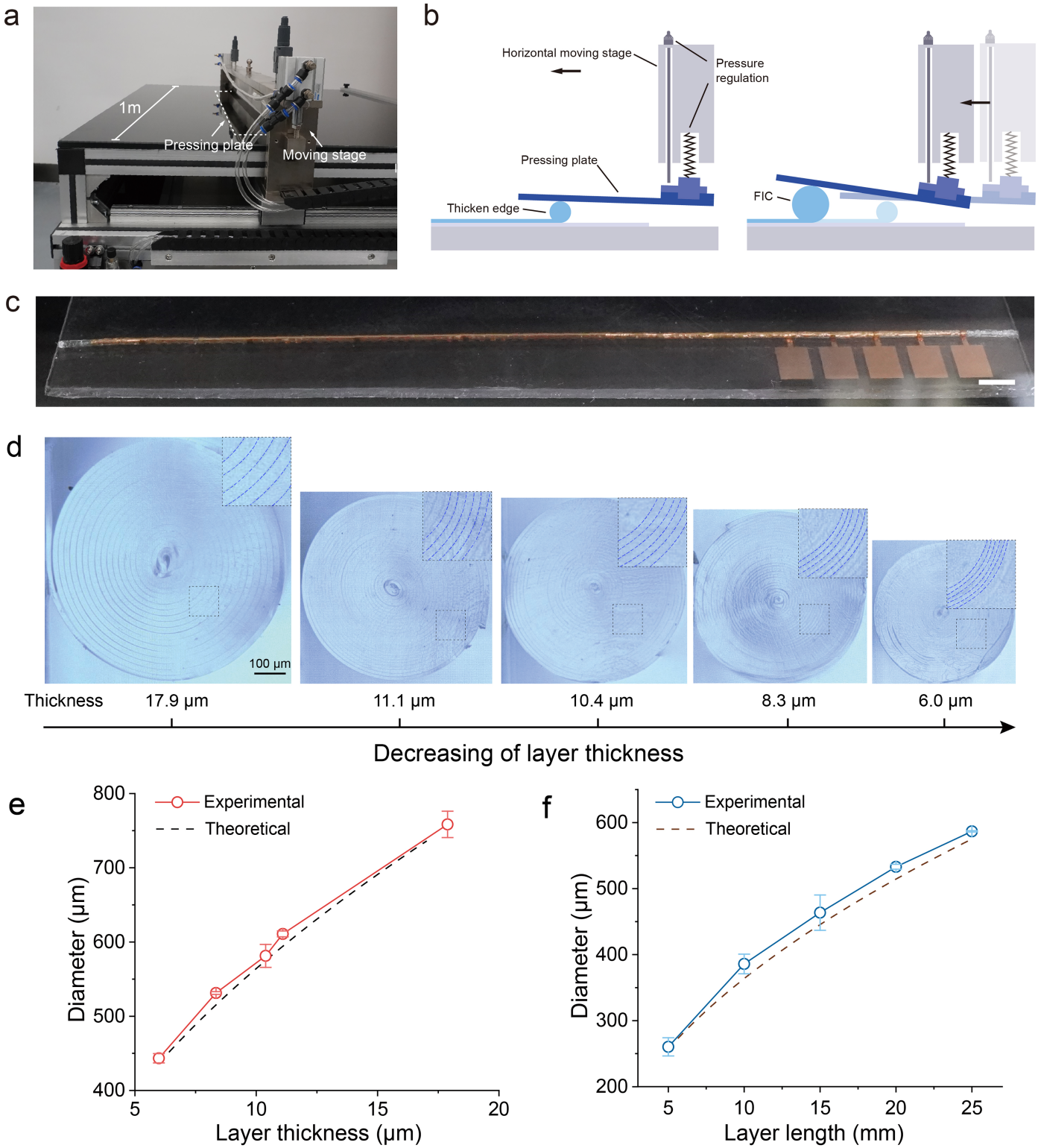
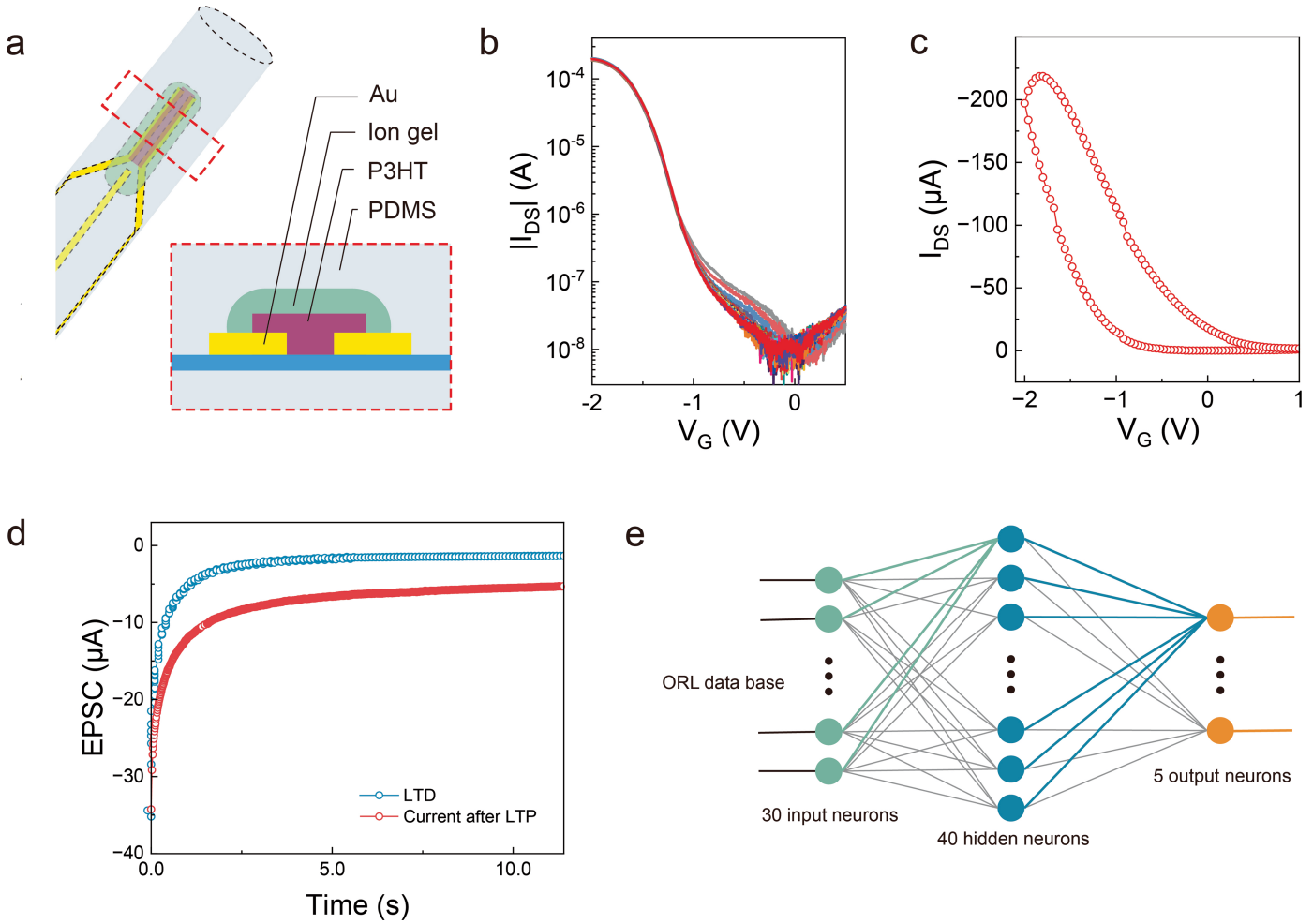


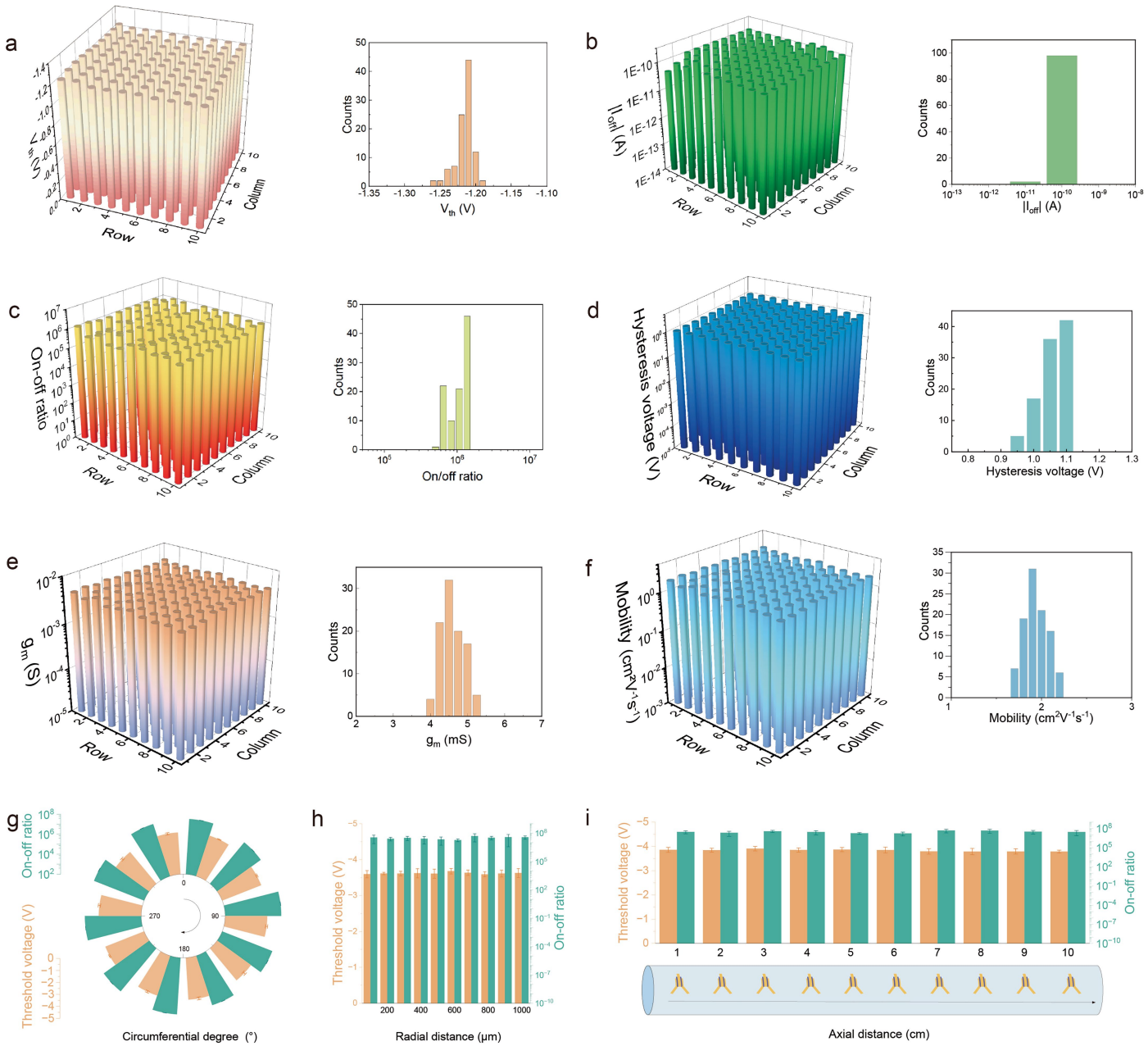
Extended Data Fig. 1 | Compact rolling of FICs. a, Reconstructed three-dimensional fluorescence photomicrograph showing the details of the multilayered device in FICs. No obvious wrinkling or distortion occurred. The volumetric integration density can increase by more than 50 times without increasing the fibre radius by using a multilayered structure, with a typical fibre diameter of 500 μm and a layer thickness of 5 μm. **b**, Photographs showing the FIC without thickened edge exhibiting random wrinkles at the beginning of the assembly process (lower image). **c**, Photographs showing the FIC without semi-cured layer exhibiting layer delamination after cyclic bending. **d**, Sectional photograph of a FIC showing the PDMS thickening region, which could locally increase the bending stiffness and inhibit the formation of wrinkles during the rolling process. Scale bar, 40 μm. **e**, Sectional photograph of a FIC showing reliable interfacial adhesion realized by applying a semi-cured PDMS layer, which contacted the PDMS substrate during the rolling process and was cured to realize adhesion. Scale bar, 10 μm. **f**, A substantial enhancement of the interlayer peeling stress was observed after a semi-cured PDMS layer was applied. **g**, Optical microscope image showing no signs of peeling or cracking after being placed in an ambient environment for one month. Scale bar, 200 μm.



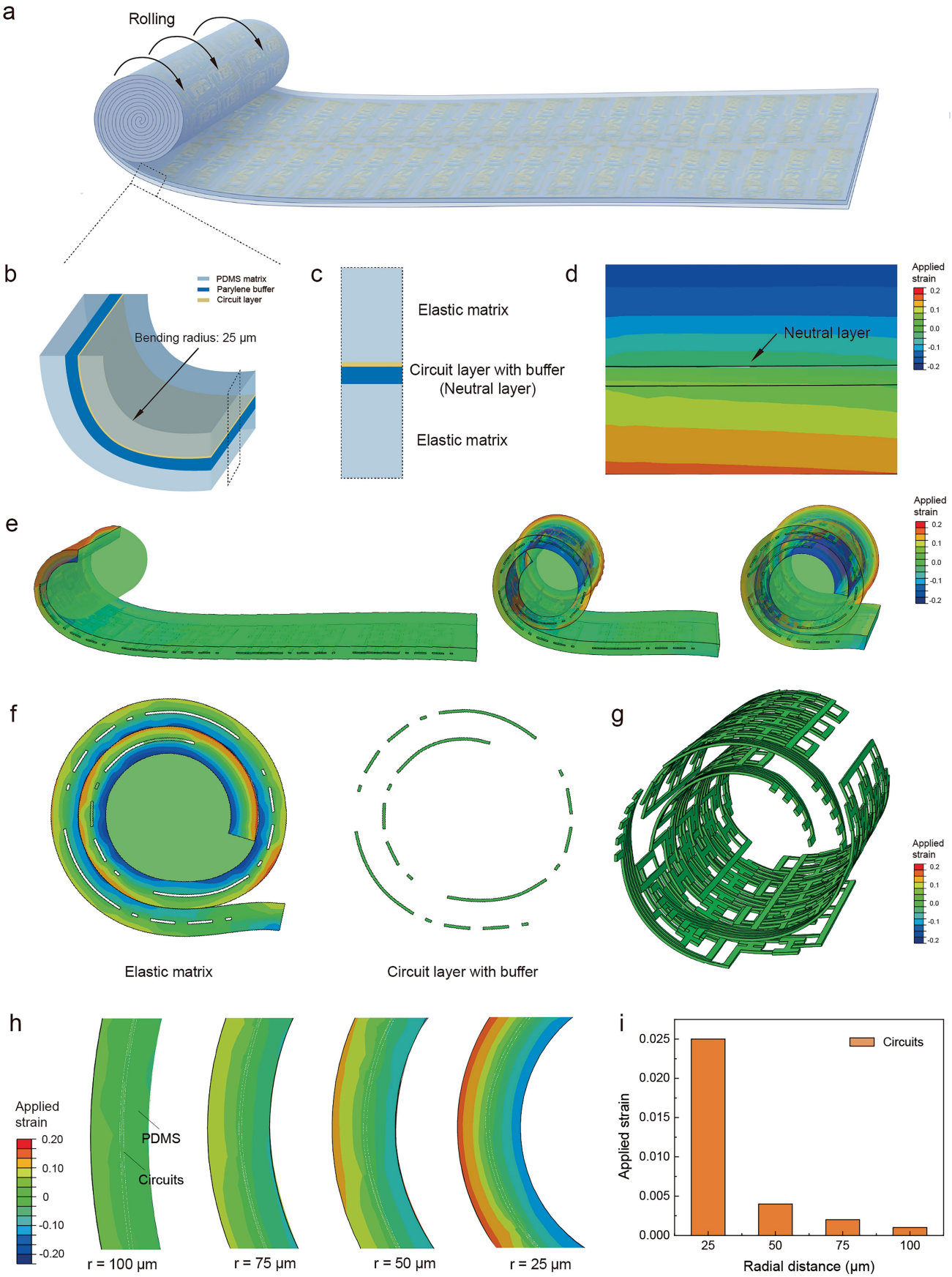
Extended Data Fig. 2 | Controllable preparation of FICs of different diameters with compact rolling. a, Photograph showing the custom-built apparatus with the fabrication length of 1 m. **b**, Schematic showing the rolling process of FICs, in which the glass pressing plate was uniformly pushed by the translation stage. By precisely adjusting the downward pressure of the pressing plate and the moving speed of the translation stage, the apparatus can stably drive the rotational rolling of FICs. **c**, Zoomed-in photograph showing the uniformly rolled FICs. Scale bar, 4 mm. **d**, Optical section photographs showing that the diameter of FICs can increase with increasing layer thickness. Scale bar, 100 μm. **e**, Statistical diagram showing that the measured diameter of the FICs is consistent with the theoretical calculation, indicating that the diameter of the device can be precisely controlled by the layer thickness. **f**, Statistical diagram showing that the measured diameter of the FICs is consistent with the theoretical calculation, indicating that the diameter of the device can be precisely controlled by the layer length. Error bars are standard deviations of the results from at least four samples.



Extended Data Fig. 3 | Neural computing capabilities of OECTs in FICs. **a**, Schematic showing the structural design of OECTs in FICs. **b**, Transition curves of 20 OECTs in FICs selected from the same batch. **c**, Transition curve of OECTs in FICs. **d**, The excitatory post-synaptic current level after long-term potentiation and long-term depression testing. **e**, Schematic of the simulated framework of a neural network constructed from OECTs. **f**, Schematic showing the simulated framework of a single-layer neural network. **g**, Simulation accuracy when testing 1,000 images in the Olivetti Research Laboratory face database. **h**, Confusion matrix showing that each digit image was optimally recognized.

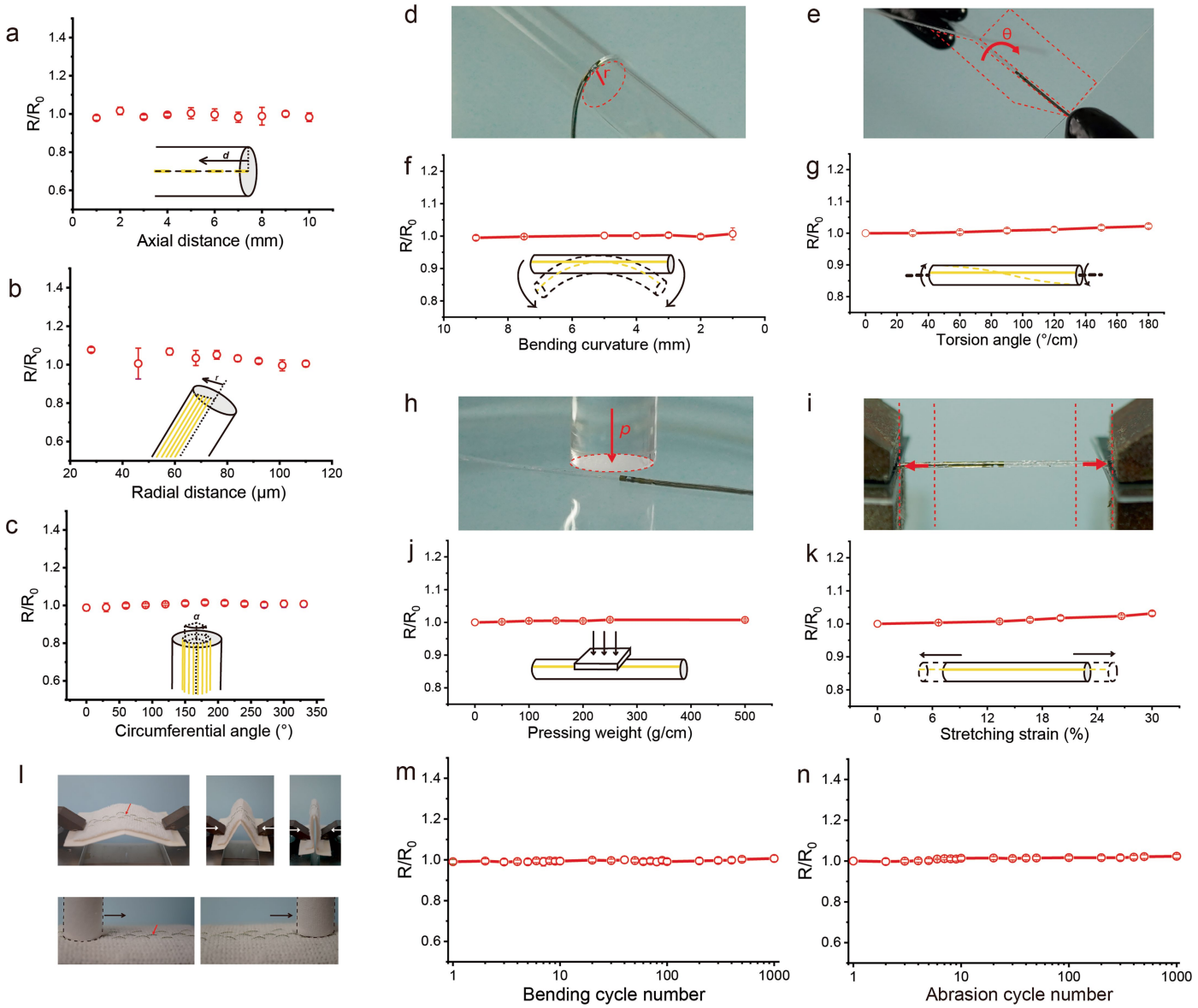


Extended Data Fig. 4 | Electrical performance uniformity of transistors in FICs. a–f, Columnar statistics of the threshold voltage, on–off ratio, off-current, transconductance, hysteresis voltage and mobility of 100 OECTs prepared in the same batch, showing minor variations in their electrical properties. **g**, Variation of transistor performances along the circumferential direction. **h**, Variation of transistor performances along the radial direction. **i**, Variation of transistor performances along the axial direction. Error bars are standard deviations of the results from at least four samples.

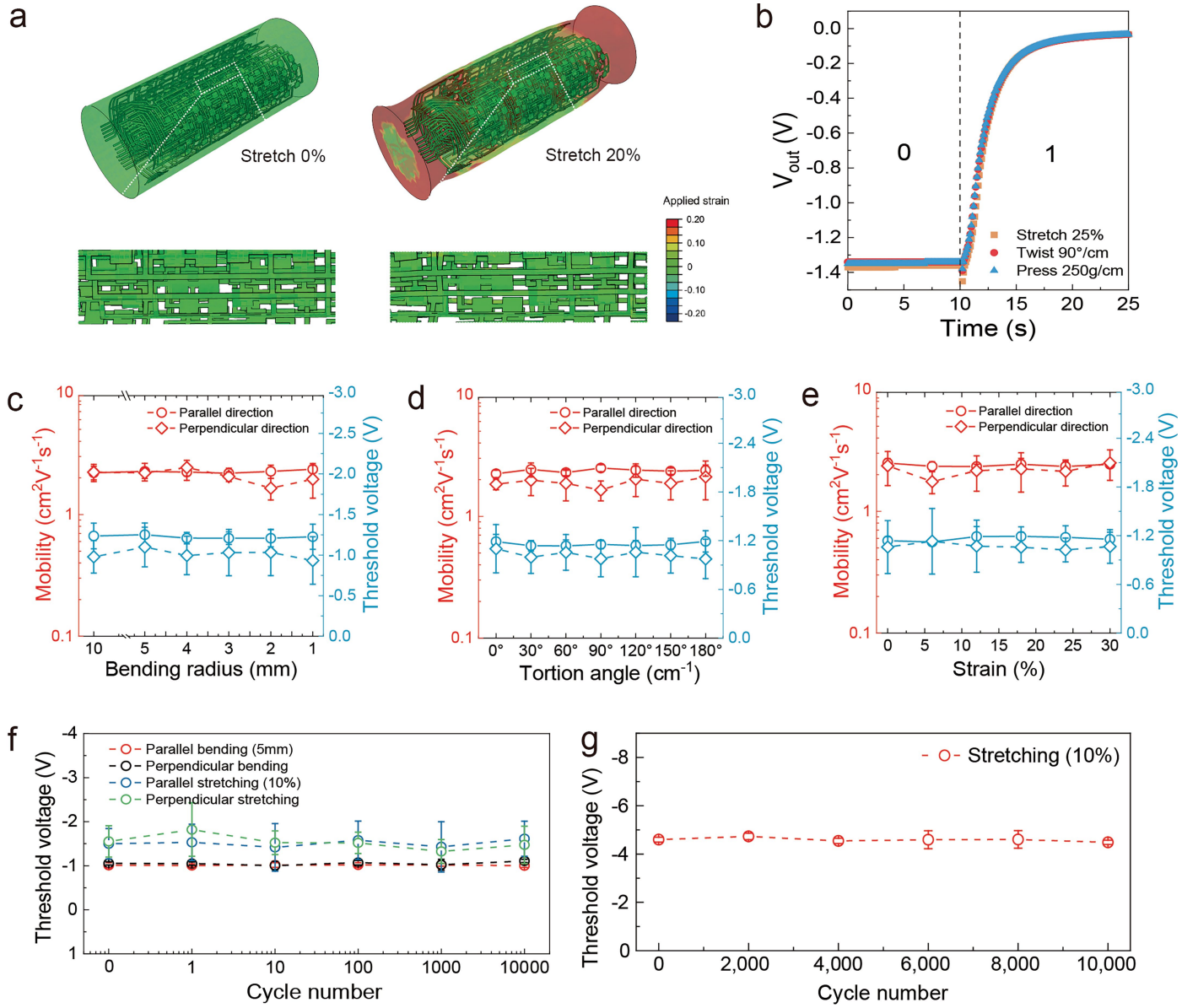


Extended Data Fig. 5 | See next page for caption.

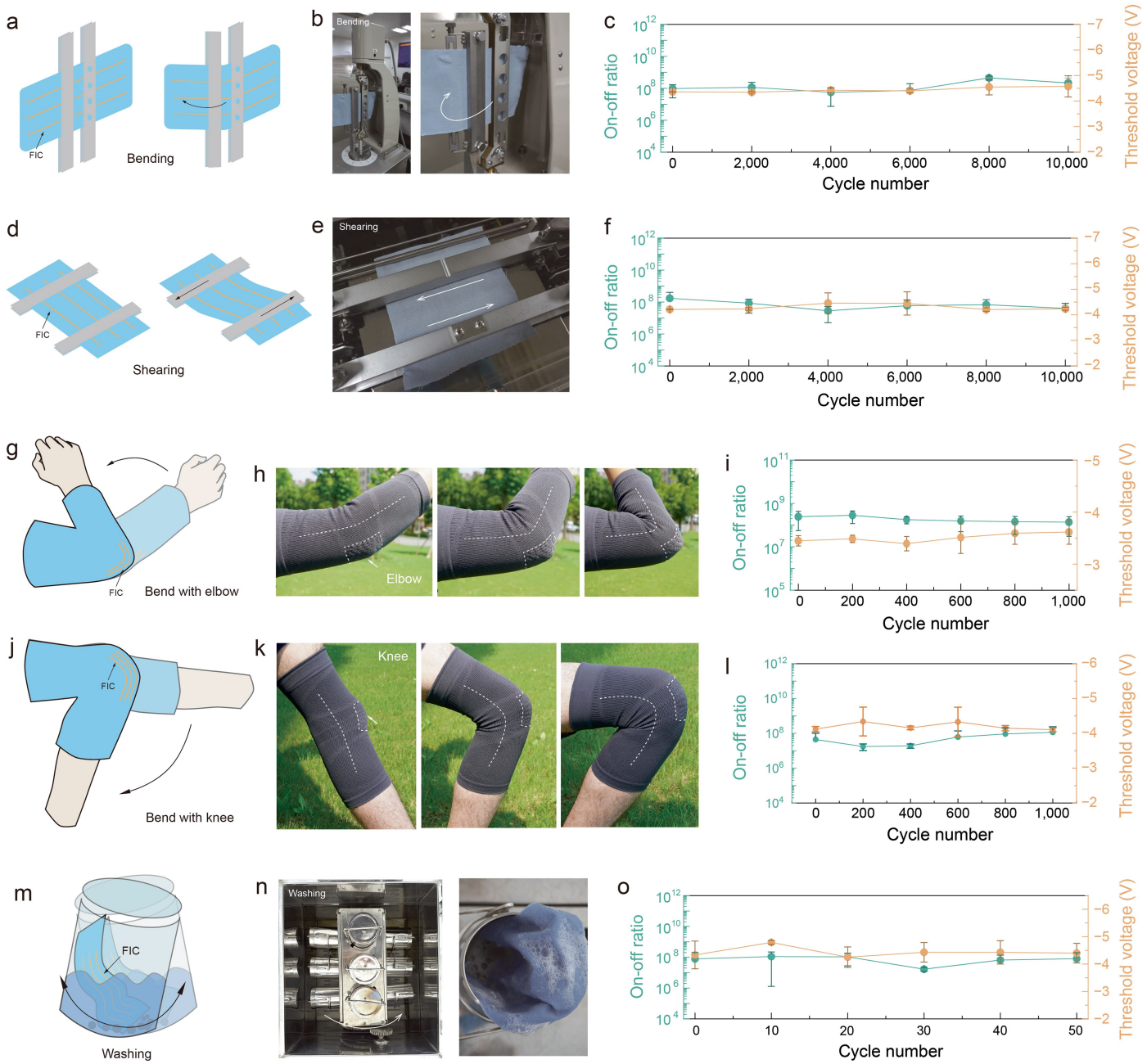
Extended Data Fig. 5 | Strategy to mitigate stress concentration during rolling. a, Schematic showing the rolling process of FICs in which the functional circuit layer is sandwiched between elastic substrates. **b**, Zoomed-in schematic showing the circuit layer located in the middle of the film during rolling. **c**, Zoomed-in schematic showing the cross-section of the film during rolling. **d**, Finite element simulation results showing that the circuit layer with buffer undergoes small strain during rolling because they were located in the neutral layer. **e**, Finite element simulation results showing the rolling process. **f**, Finite element simulation results showing that no obvious strain concentration occurs in the cross-section of the functional circuit layer after rolling. **g**, Finite element simulation results showing that no obvious strain concentration occurs in the functional circuit layers after rolling. **h**, Finite element simulation results showing the strain distribution of the circuit located at incremental distances from the fibre core. **i**, Statistical histogram showing the applied strain on the PDMS matrix and circuits in layers of different radial distances.



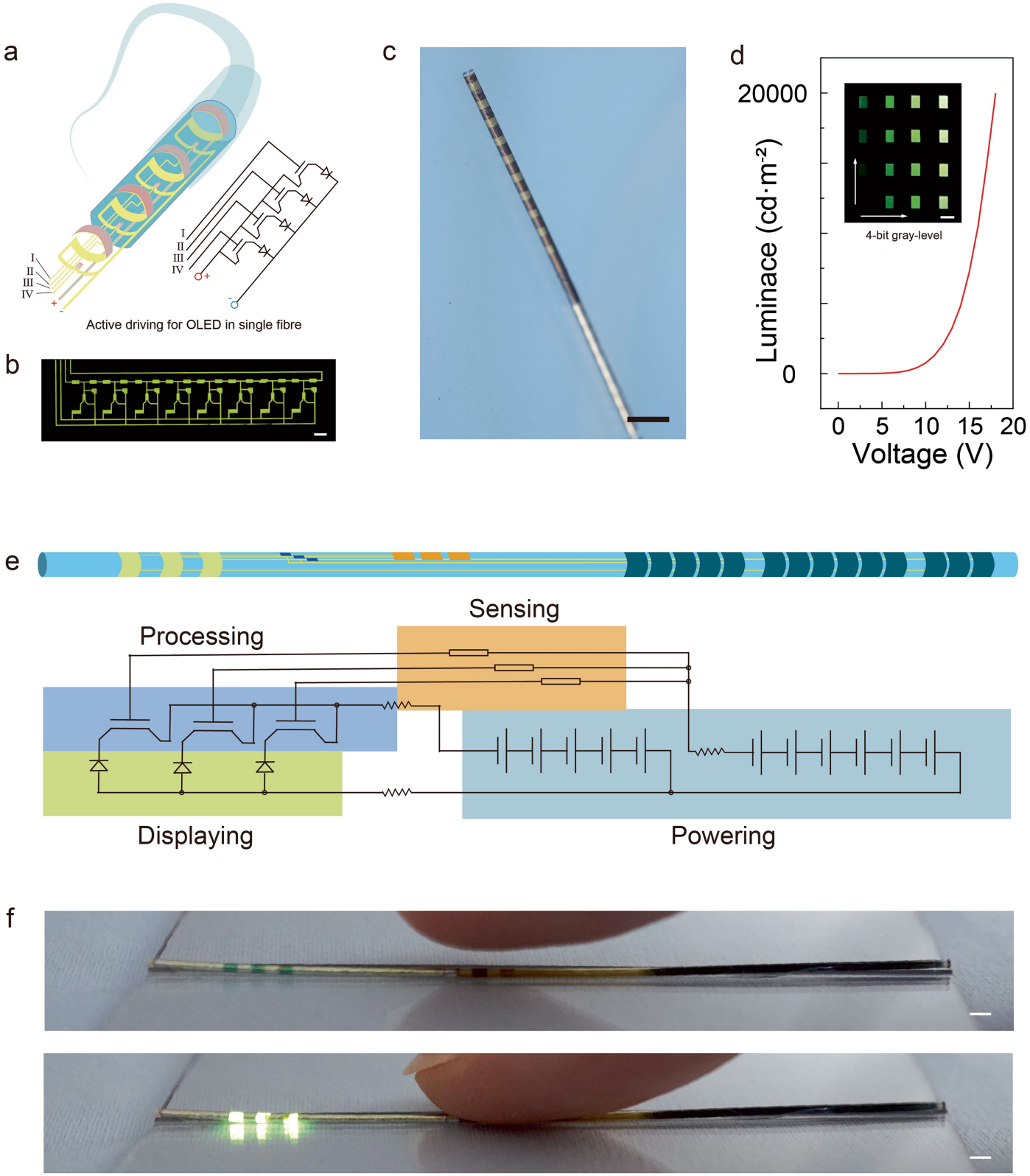
Extended Data Fig. 6 | Stability and durability of the conductive tracks in FICs. a, Resistance variation of metal pathways in FICs along the axial direction. **b**, Resistance variation of metal pathways in FICs along the radial direction. **c**, Resistance variation of metal pathways in FICs along the circumferential direction. **d**, Photograph showing the metal pathways in a FIC bent around a cylinder with a specific radius. **e**, Photograph showing the metal pathways in a FIC twisted at a specific angle. **f**, Resistance variation of metal pathways in FICs when bent with different curvatures. **g**, Resistance variation of metal pathways in FICs when twisted at different angles. **h**, Photograph showing the metal pathways in a FIC pressed by a cylinder with a specific weight. **i**, Photograph showing the metal pathways in a FIC stretched to a specific strain. **j**, Resistance variation of metal pathways in FICs when pressed with different weights. **k**, Resistance variation of metal pathways in FICs when stretched to different strains. **l**, Photograph showing the metal pathways in FICs tested by means of bending and abrasion cycles. **m**, Resistance variation of metal pathways in FICs during 1,000 bending cycles. **n**, Resistance variation of metal pathways in FICs during 1,000 abrasion cycles. Error bars are standard deviations of the results from at least four samples.



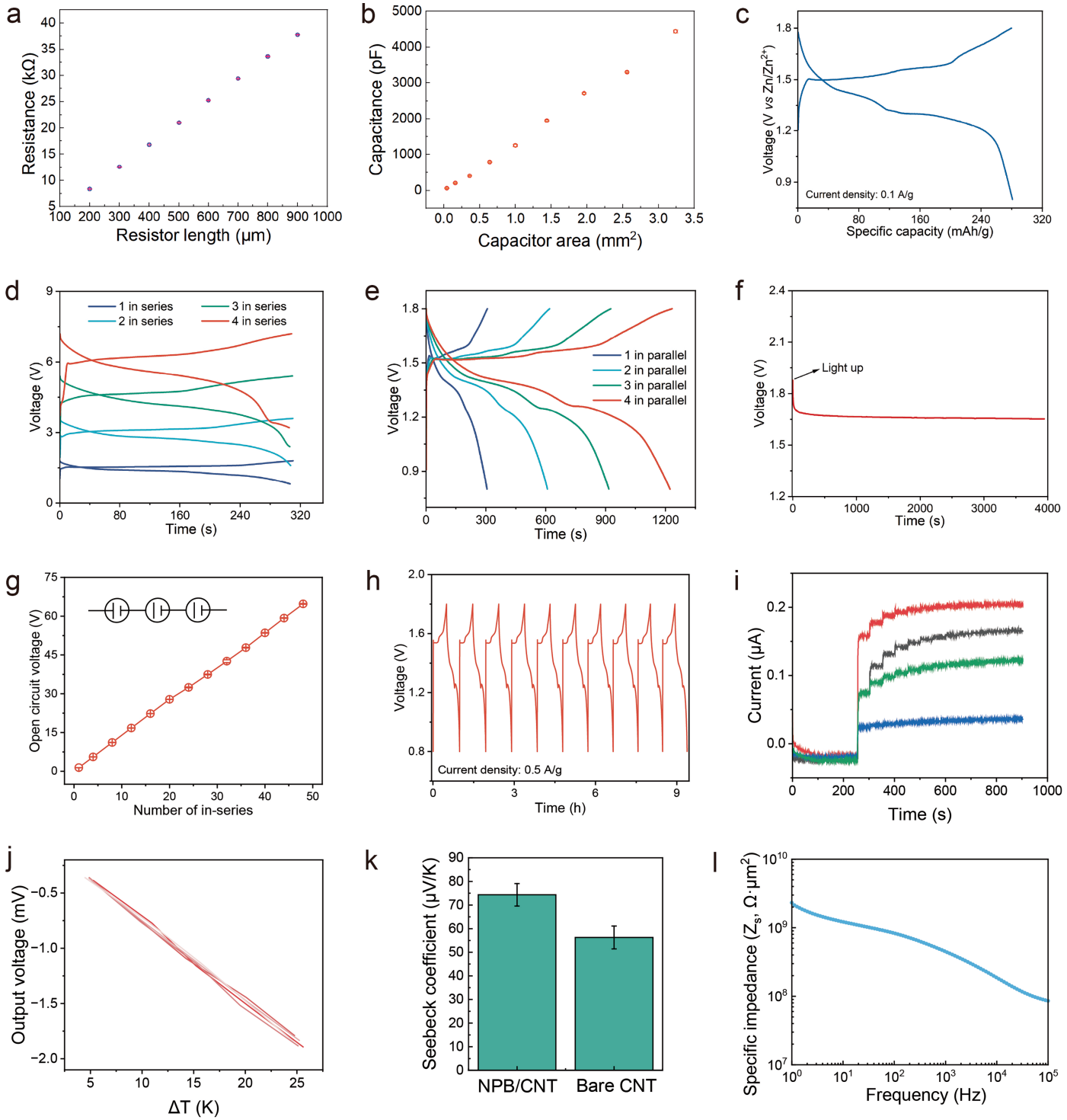
Extended Data Fig. 7 | Stability and durability of transistors in FICs. a, Finite element simulation results showing the strain distributions of a realistic highly integrated FIC when stretched towards 20%. **b**, Statistical diagram of the output from OECTs in a FIC during stretching, twisting and pressing. **c**, Statistical diagram of the mobility and threshold voltage of OECTs in a FIC during bending with different bending radii. **d**, Statistical diagram of the mobility and threshold voltage of OECTs in a FIC during twisting with different torsion angles. **e**, Statistical diagram of the mobility and threshold voltage of OECTs in a FIC during stretching with different strains. **f**, Statistical diagram of the threshold voltage of OECTs in a fibre during 10,000 bending and stretching cycles. **g**, Statistical diagram of the threshold voltage of transistors in a fibre during 10,000 stretching cycles. Error bars are standard deviations of the results from at least four samples.



Extended Data Fig. 8 | Practical stability of FICs. a, Schematic showing the FIC textile being bent 90° for 1,000 cycles. **b**, Photograph showing the FIC textile being sheared on a standard bending tester. **c**, Performance variation of transistors in the FIC during 1,000 bending cycles. **d**, Schematic showing the FIC textile being sheared 10° for 1,000 cycles. **e**, Photograph showing the FIC textile being sheared in a Kawabata evaluation system. **f**, Performance variation of transistors in FICs during 1,000 shearing cycles. **g**, Schematic showing the FICs being bent 90° in the elbow part of a sleeve for 1,000 cycles. **h**, Photograph showing the FICs in a sleeve being bent by an arm. **i**, Performance variation of transistors in the FICs during 1,000 bending cycles. **j**, Schematic showing the FICs being bent 90° in a knee pad for 1,000 cycles. **k**, Photograph showing the FICs in a knee pad being bent by a leg. **l**, Performance variation of transistors in the FICs during 1,000 bending cycles. **m**, Schematic showing the FIC textile being washed for 50 cycles. **n**, Photograph showing the FIC being washed in a standard washing machine. **o**, Performance variation of transistors in the FICs during 50 washing cycles. Error bars are standard deviations of the results from at least four samples.



Extended Data Fig. 9 | Performance of OLEDs in FICs. a, Schematic showing the structural design of OLEDs and active driving circuits in intelligent fibre systems. **b**, Photograph showing the morphology of fluorescent-labelled active driving circuits in intelligent fibre systems. Scale bar, 100 μm. **c**, Photograph showing the display module in intelligent fibre systems. Scale bar, 1 mm. **d**, Brightness of a single luminescent pixel in intelligent fibre systems being controlled by the applied input voltage. Inset, photograph showing that the active driving circuit in intelligent fibre systems can control pixels to display a 4-bit grey level. Scale bar, 1 mm. **e**, Schematic showing the circuit design of a closed-loop fibre system including power, sensing, signal-processing and displaying modules. **f**, Photograph showing the fibre system in which the displaying module can be controlled by touching the sensing point in the middle of the fibre. Scale bar, 2 mm.



Extended Data Fig. 10 | Performance of other functional units in FICs. **a**, Resistances of resistors in a fibre showing linearity with increasing length of the resistive pattern. **b**, Capacitance of capacitors in a fibre showing linearity with increasing electrode overlap area. **c**, Galvanostatic charge-discharge curves of batteries in intelligent fibre systems. **d**, Galvanostatic charge-discharge profiles of batteries in intelligent fibre systems connected in series. **e**, Galvanostatic charge-discharge profiles of batteries in intelligent fibre systems connected in parallel. **f**, Voltage outputs of batteries in intelligent fibre systems after a light-emitting diode is lit up. **g**, Statistics showing that open-circuit voltage varied with the increasing number of in-series battery units. **h**, Charge–discharge performance of the energy-storage module in FICs with a current density of 0.5 A g^{-1}. **i**, Current output of a glucose electrochemical sensor in intelligent fibre systems. **j**, Thermoelectric output voltage of thermoelectric units according to the temperature difference. **k**, Comparison of the Seebeck coefficient between CNT oriented Ni-polymer units with that of traditional CNT thermoelectric devices. **l**, Specific impedance of an electrophysiological sensor in intelligent fibre systems. Error bars are standard deviations of the results from at least four samples.

nature portfolio

Corresponding author(s): Peining Chen, and Huisheng Peng

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Our web collection on statistics for biologists contains articles on many of the points above.

Software and code

Policy information about availability of computer code

Data collection	BlackRock Microsystems
Data analysis	Spike 2 (CED)

For manuscripts utilizing custom algorithms or software that are central to the research but not yet described in published literature, software must be made available to editors and reviewers. We strongly encourage code deposition in a community repository (e.g. GitHub). See the Nature Portfolio guidelines for submitting code & software for further information.

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The data that support the findings of this study are available from figshare at
673 https://figshare.com/s/49d5ed422b56a22dda21.

Research involving human participants, their data, or biological material

Policy information about studies with human participants or human data. See also policy information about sex, gender (identity/presentation), and sexual orientation and race, ethnicity and racism.

Reporting on sex and gender	N/A
Reporting on race, ethnicity, or other socially relevant groupings	N/A
Population characteristics	N/A
Recruitment	N/A
Ethics oversight	N/A

Note that full information on the approval of the study protocol must also be provided in the manuscript.

Field-specific reporting

Please select the one below that is the best fit for your research. If you are not sure, read the appropriate sections before making your selection.

☒ Life sciences ☐ Behavioural & social sciences ☐ Ecological, evolutionary & environmental sciences

For a reference copy of the document with all sections, see nature.com/documents/nr-reporting-summary-flat.pdf

Life sciences study design

All studies must disclose on these points even when the disclosure is negative.

Sample size	We chose the sample size of n=3 for nude mice.
Data exclusions	No data were excluded from this study.
Replication	All experiments were reliably reproduced using more than 3 technical repeats, and the success rate of implantation was over 95%. All conclusions were reproducible from these experiments.
Randomization	To verify fidelity of sensors of fibre integrated circuits, nude mice were randomly selected for neural signal acquisition.
Blinding	Blinding was not performed, because there was no subjective test in this study.

Behavioural & social sciences study design

All studies must disclose on these points even when the disclosure is negative.

Study description	
Research sample	
Sampling strategy	
Data collection	
Timing	
Data exclusions	
Non-participation	
Randomization	

Ecological, evolutionary & environmental sciences study design

All studies must disclose on these points even when the disclosure is negative.

Study description	
Research sample	
Sampling strategy	
Data collection	
Timing and spatial scale	
Data exclusions	
Reproducibility	
Randomization	
Blinding	

Did the study involve field work? ☐ Yes ☐ No

Field work, collection and transport

Field conditions	
Location	
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We require information from authors about some types of materials, experimental systems and methods used in many studies. Here, indicate whether each material, system or method listed is relevant to your study. If you are not sure if a list item applies to your research, read the appropriate section before selecting a response.

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☒	☐ Antibodies
☒	☐ Eukaryotic cell lines
☒	☐ Palaeontology and archaeology
☐	☒ Animals and other organisms
☒	☐ Clinical data
☒	☐ Dual use research of concern
☒	☐ Plants

Methods

n/a	Involved in the study
☒	☐ ChIP-seq
☒	☐ Flow cytometry
☒	☐ MRI-based neuroimaging

Antibodies

Antibodies used	
Validation	

Eukaryotic cell lines

Policy information about cell lines and Sex and Gender in Research

Cell line source(s)	
Authentication	
Mycoplasma contamination	
Commonly misidentified lines (See ICLAC register)	

Palaeontology and Archaeology

Specimen provenance	
Specimen deposition	
Dating methods	

☐ Tick this box to confirm that the raw and calibrated dates are available in the paper or in Supplementary Information.

Ethics oversight	

Note that full information on the approval of the study protocol must also be provided in the manuscript.

Animals and other research organisms

Policy information about studies involving animals; ARRIVE guidelines recommended for reporting animal research, and Sex and Gender in Research

Laboratory animals	Nude mice (ICR, 6 weeks old, about 20 g in weight, Shanghai SLAC Laboratory Animal Co., Ltd.)
Wild animals	The study did not involve wild animals.
Reporting on sex	Sex was not considered in this study.
Field-collected samples	The study did not involve samples collected from the field.
Ethics oversight	The experiment protocols were approved by the Animal Experimentation Committee of Fudan University. All animals were treated in accordance with guidelines for the care and use of experimental animals described by the National Institutes of Health and Fudan University.

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Clinical trial registration	
Study protocol	
Data collection	
Outcomes	

Dual use research of concern

Policy information about dual use research of concern

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Could the accidental, deliberate or reckless misuse of agents or technologies generated in the work, or the application of information presented in the manuscript, pose a threat to:

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☐	☐	National security
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☐	☐	Ecosystems
☐	☐	Any other significant area

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Does the work involve any of these experiments of concern:

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☐	☐	Enhance the virulence of a pathogen or render a nonpathogen virulent
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☐	☐	Alter the host range of a pathogen
☐	☐	Enable evasion of diagnostic/detection modalities
☐	☐	Enable the weaponization of a biological agent or toxin
☐	☐	Any other potentially harmful combination of experiments and agents

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Seed stocks	The study did not involve seeds or plants.
Novel plant genotypes	The study did not involve novel plant genotypes.
Authentication	The study did not involve seeds or plants.

ChIP-seq

Data deposition

☐ Confirm that both raw and final processed data have been deposited in a public database such as GEO.

☐ Confirm that you have deposited or provided access to graph files (e.g. BED files) for the called peaks.

Data access links *May remain private before publication.*	
Files in database submission	
Genome browser session (e.g. UCSC)	

Methodology

Replicates	
Sequencing depth	
Antibodies	
Peak calling parameters	

Data quality

Software

Flow Cytometry

Plots

Confirm that:

☐ The axis labels state the marker and fluorochrome used (e.g. CD4-FITC).

☐ The axis scales are clearly visible. Include numbers along axes only for bottom left plot of group (a 'group' is an analysis of identical markers).

☐ All plots are contour plots with outliers or pseudocolor plots.

☐ A numerical value for number of cells or percentage (with statistics) is provided.

Methodology

Sample preparation

Instrument

Software

Cell population abundance

Gating strategy

☐ Tick this box to confirm that a figure exemplifying the gating strategy is provided in the Supplementary Information.

Magnetic resonance imaging

Experimental design

Design type

Design specifications

Behavioral performance measures

Acquisition

Imaging type(s)

Field strength

Sequence & imaging parameters

Area of acquisition

Diffusion MRI ☐ Used ☐ Not used

Preprocessing

Preprocessing software

Normalization

Normalization template

Noise and artifact removal

Volume censoring

Statistical modeling & inference

Model type and settings

Effect(s) tested

Specify type of analysis: ☐ Whole brain ☐ ROI-based ☐ Both

Statistic type for inference

(See Eklund et al. 2016)

Correction

Models & analysis

n/a	Involved in the study
☐	☐ Functional and/or effective connectivity
☐	☐ Graph analysis
☐	☐ Multivariate modeling or predictive analysis

Functional and/or effective connectivity

Graph analysis

Multivariate modeling and predictive analysis